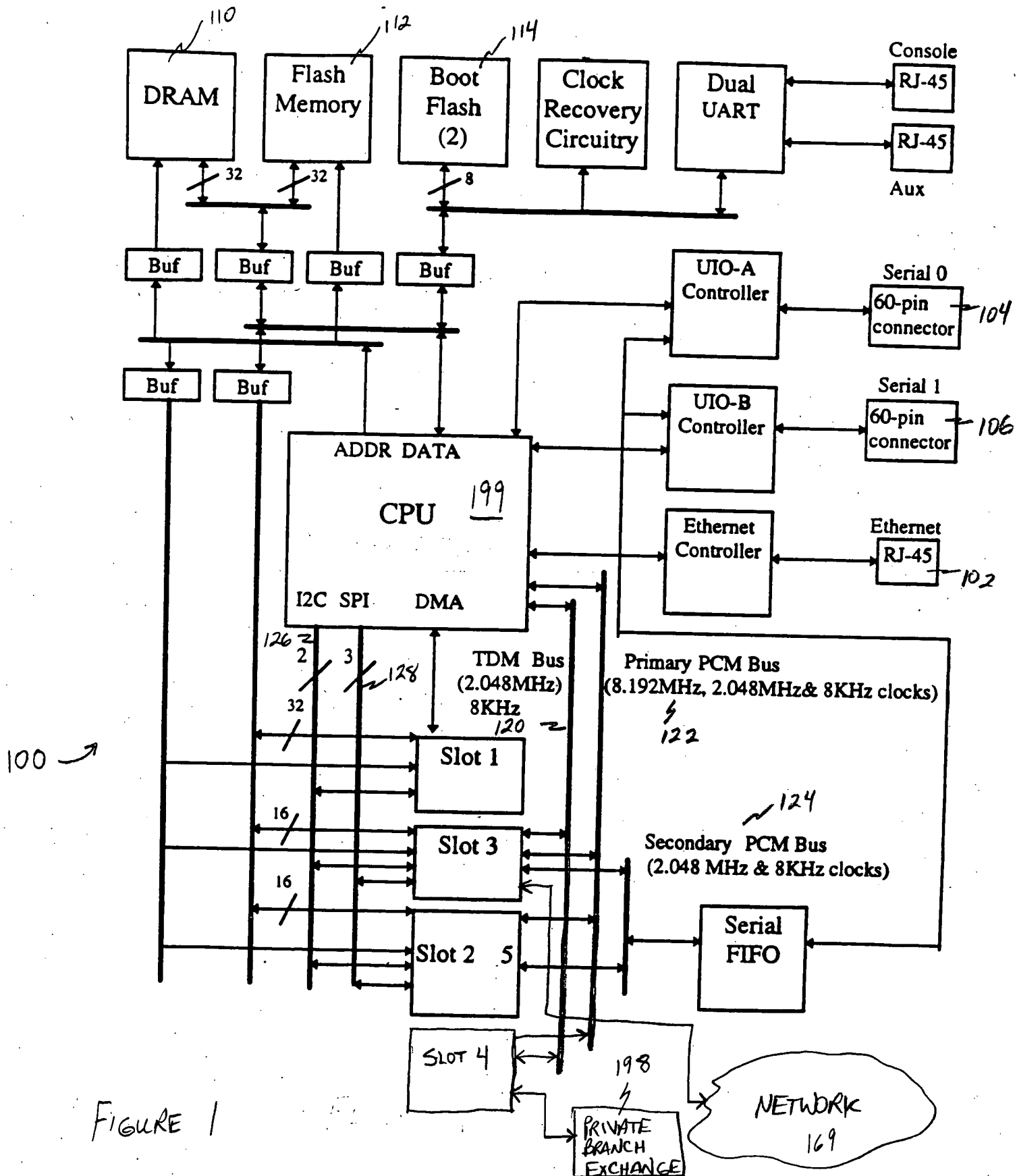


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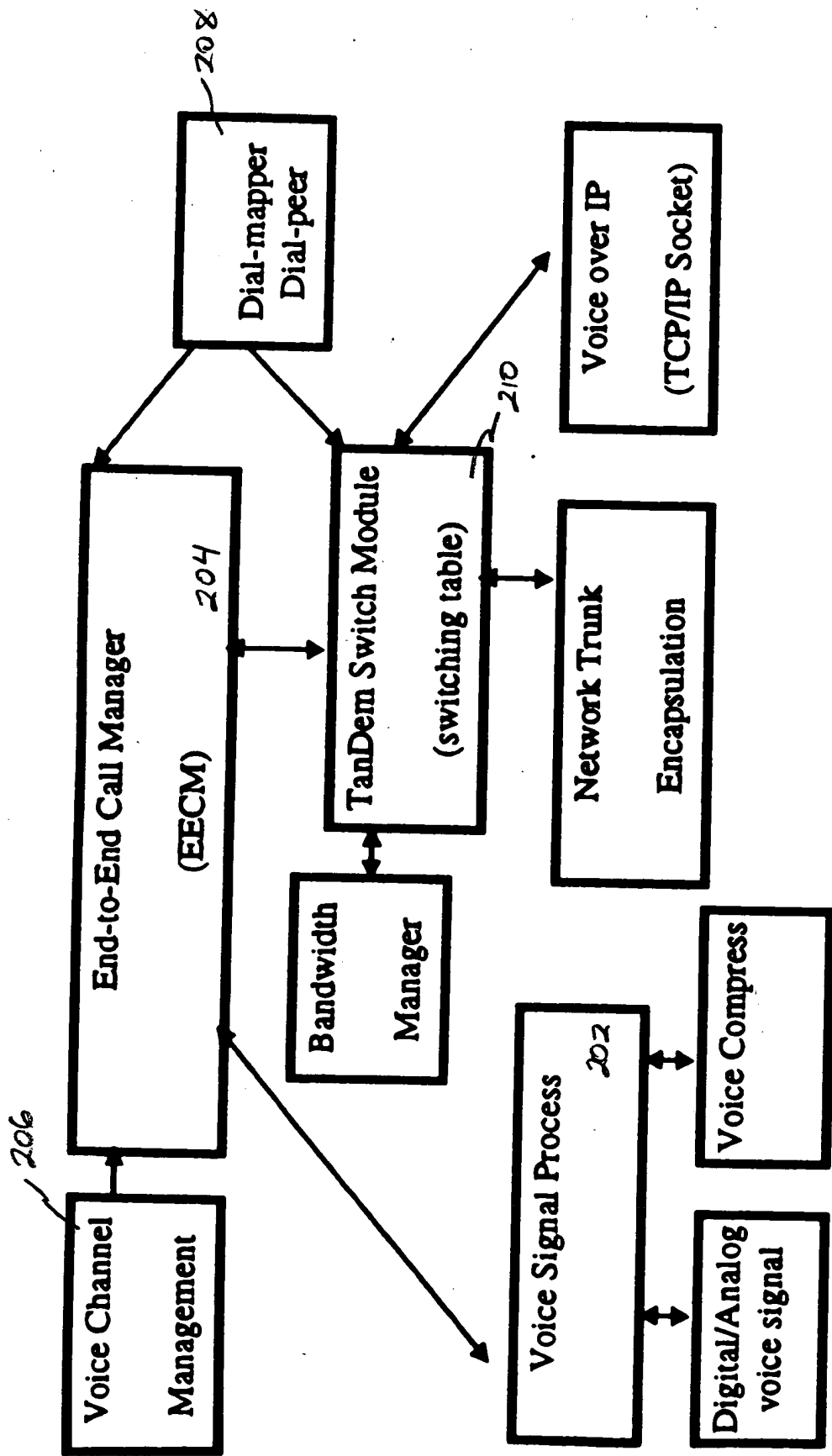


FIGURE 2

REF ID: A64496

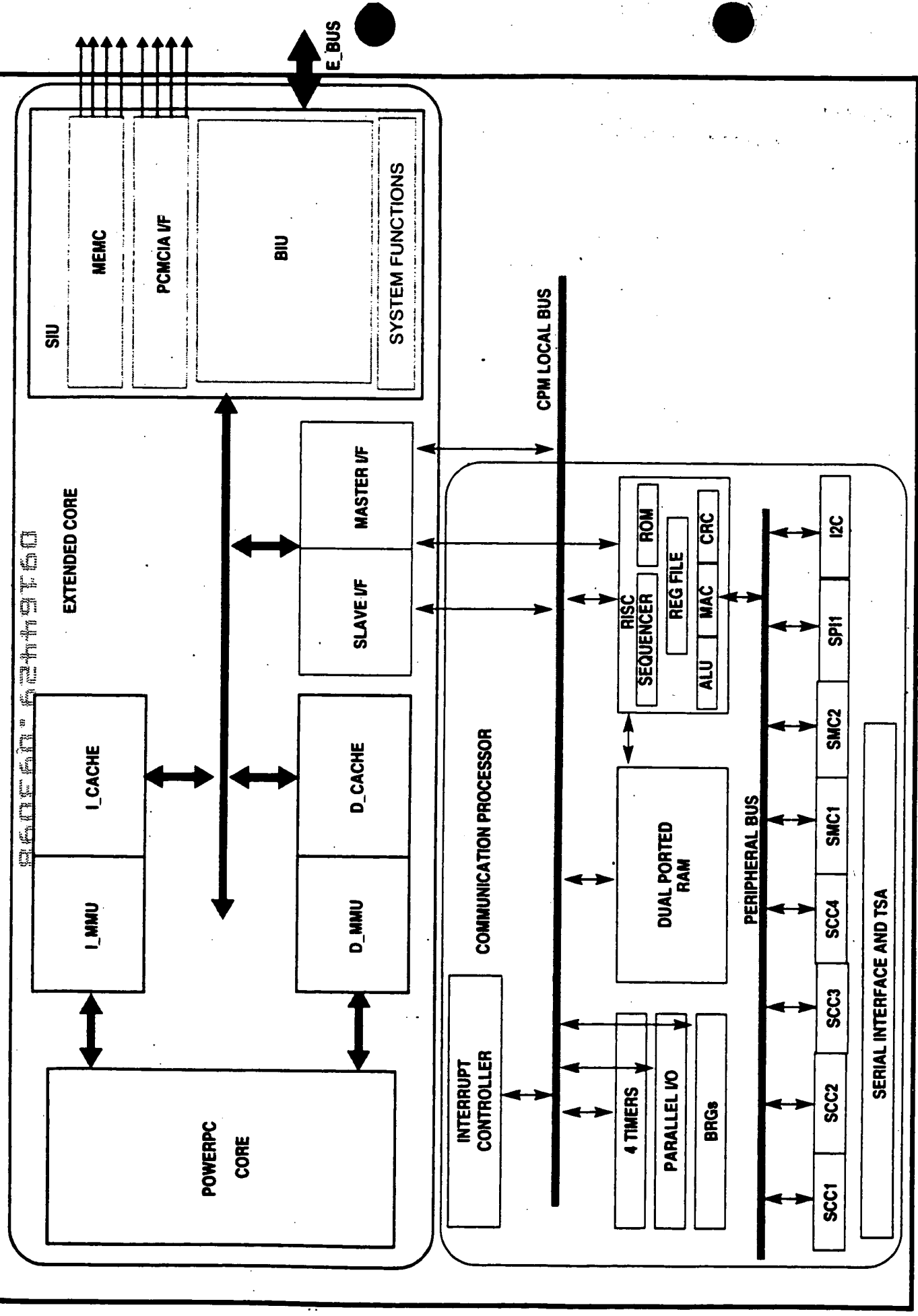


FIGURE 3

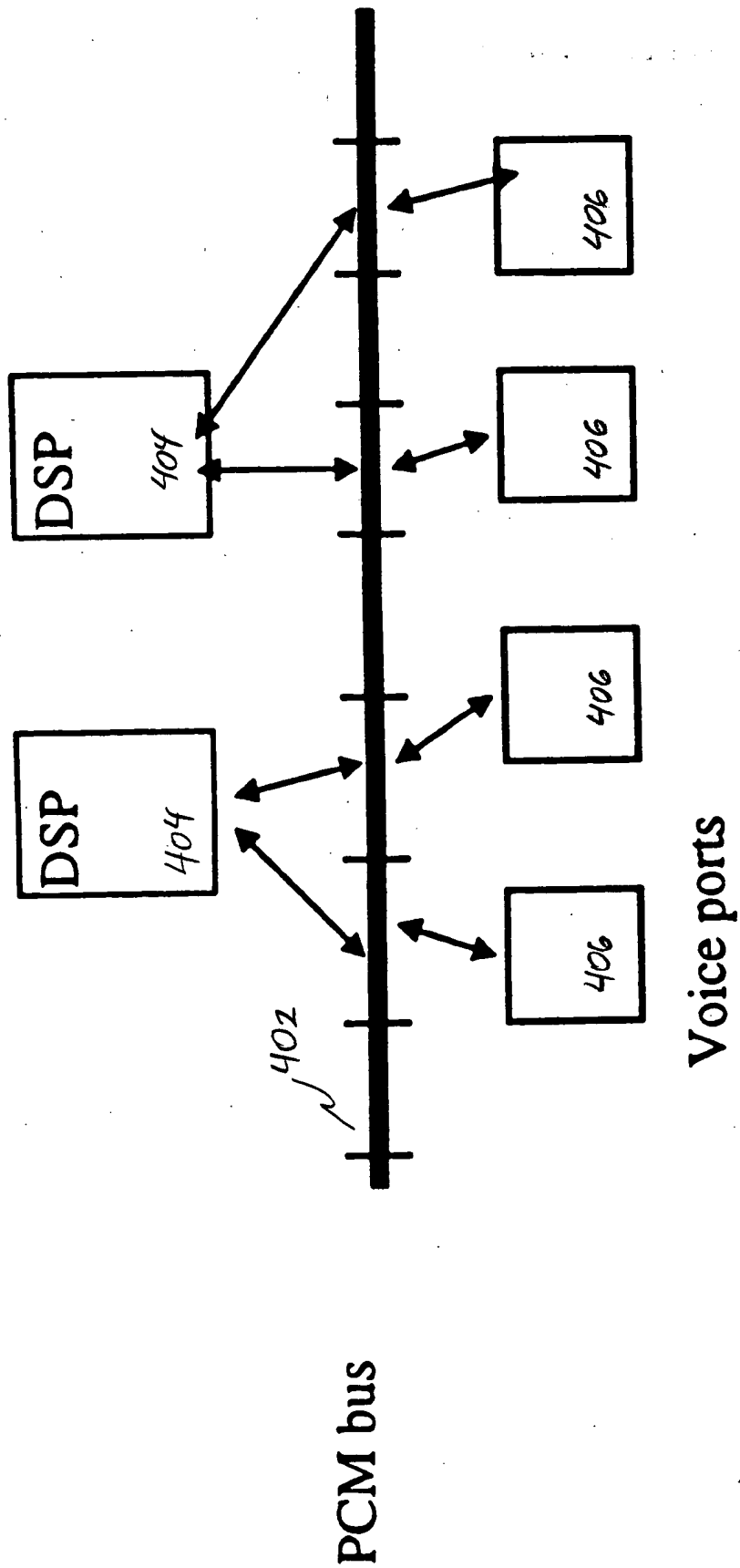


FIGURE 4

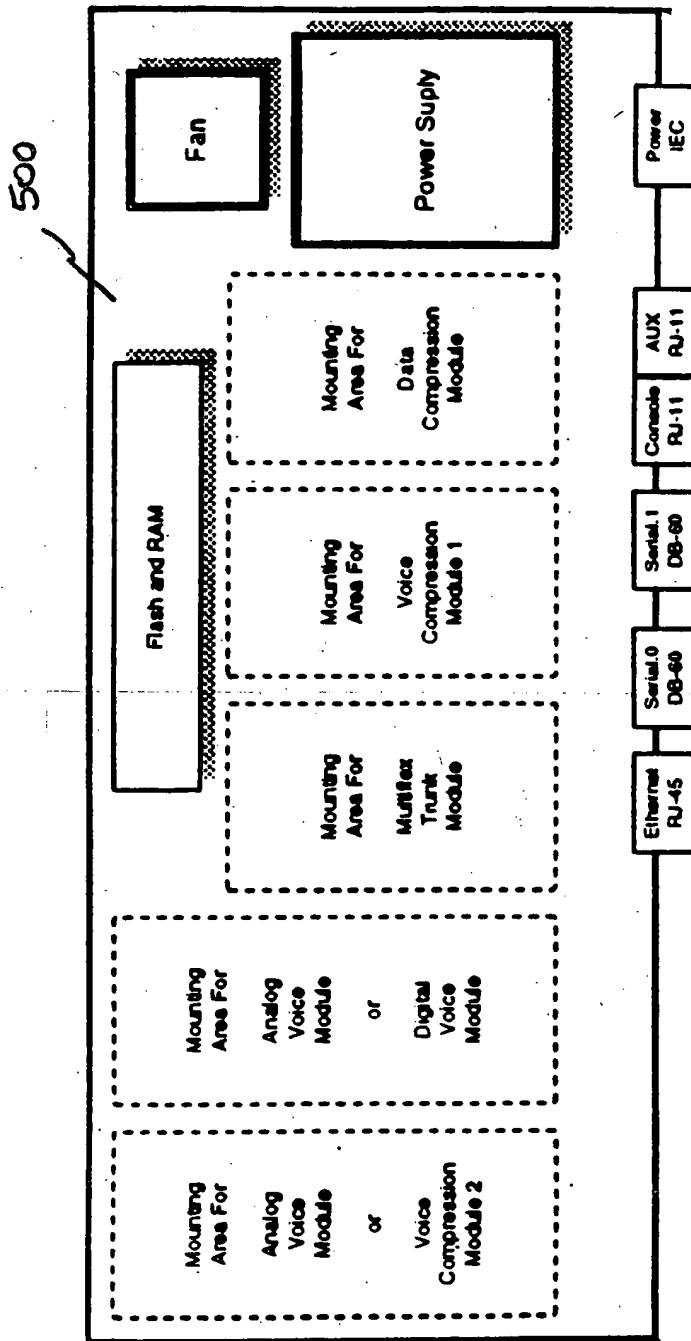


FIGURE 5

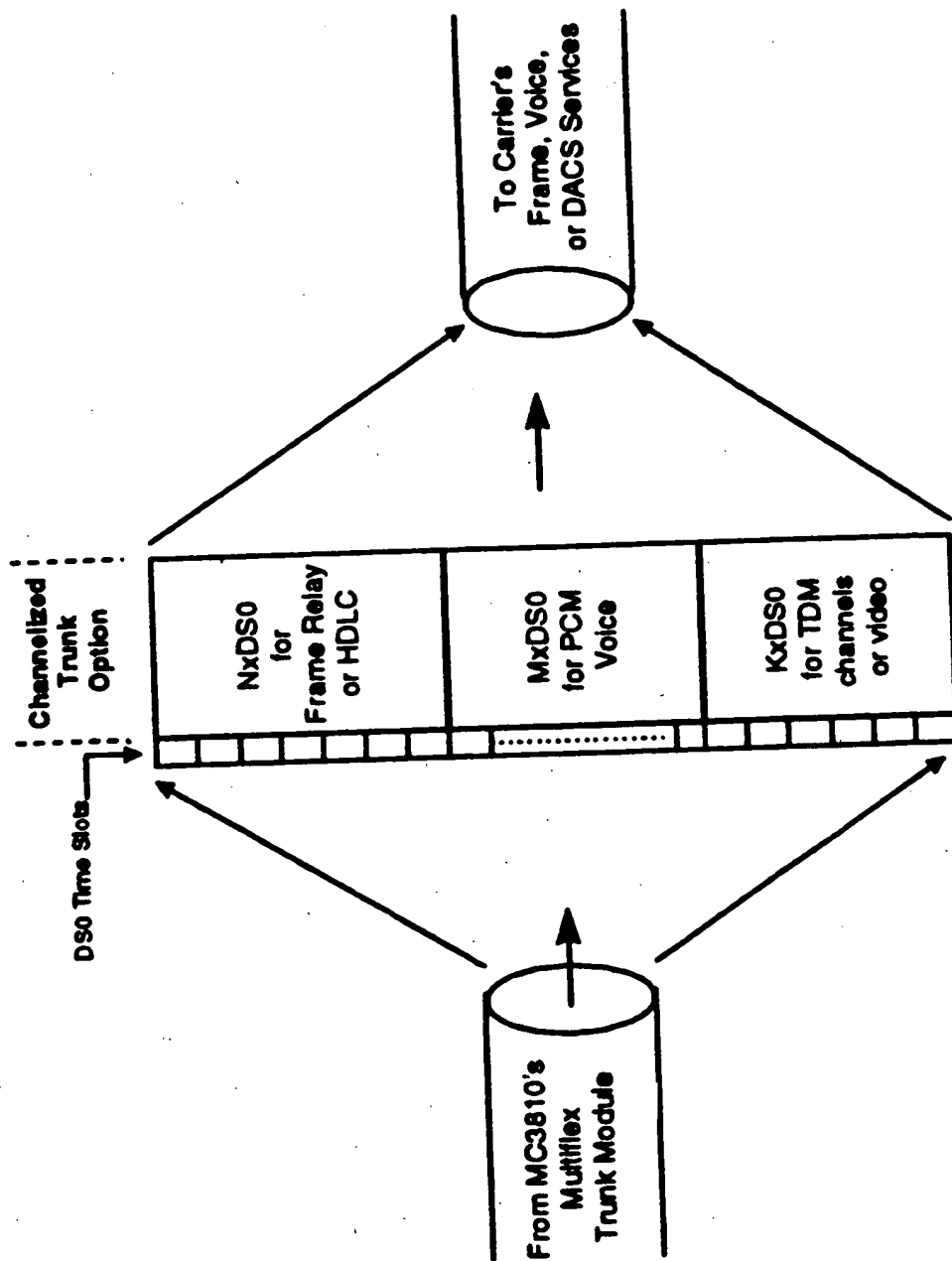


FIGURE 6

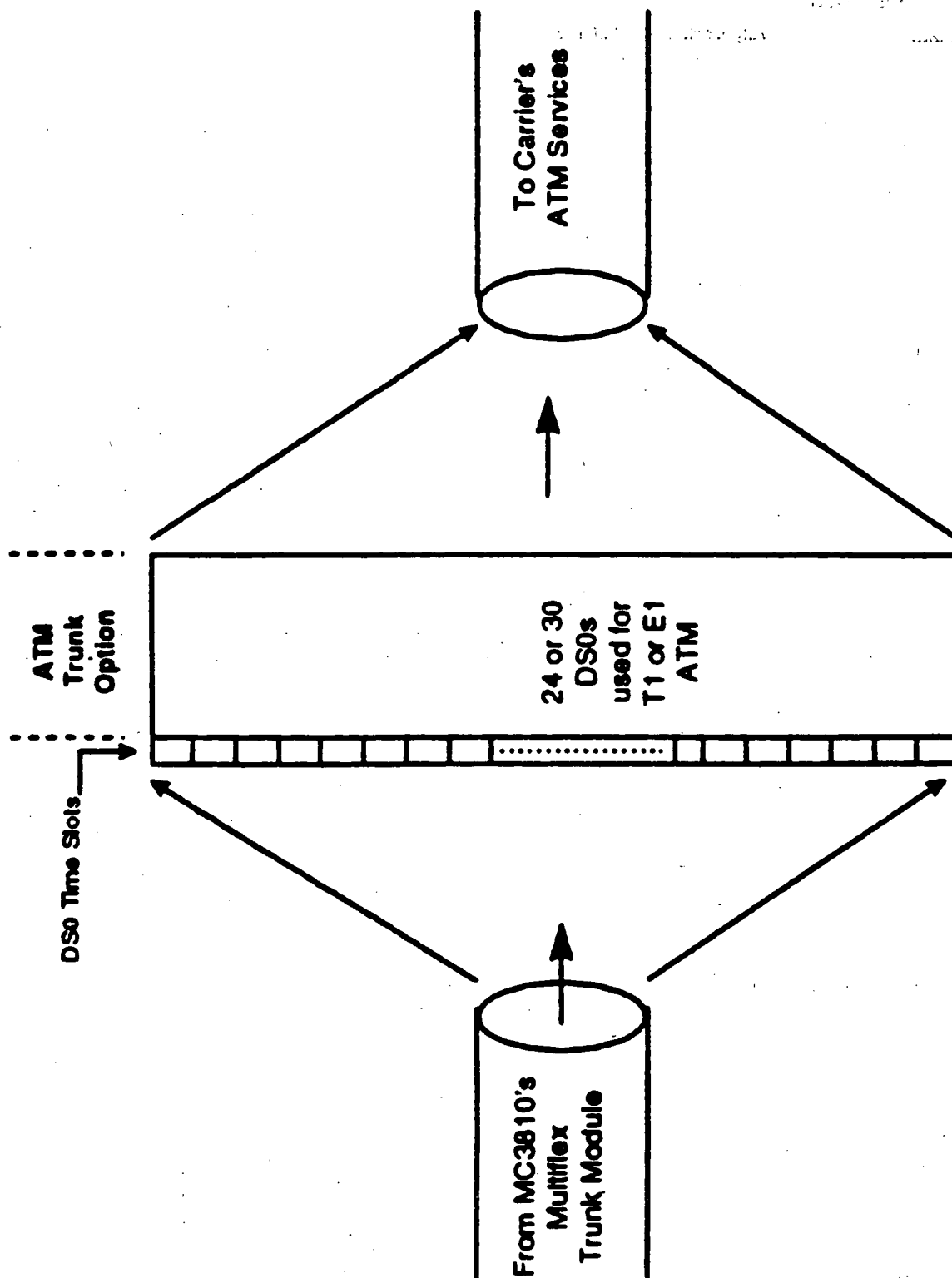


FIGURE 7

SECRET

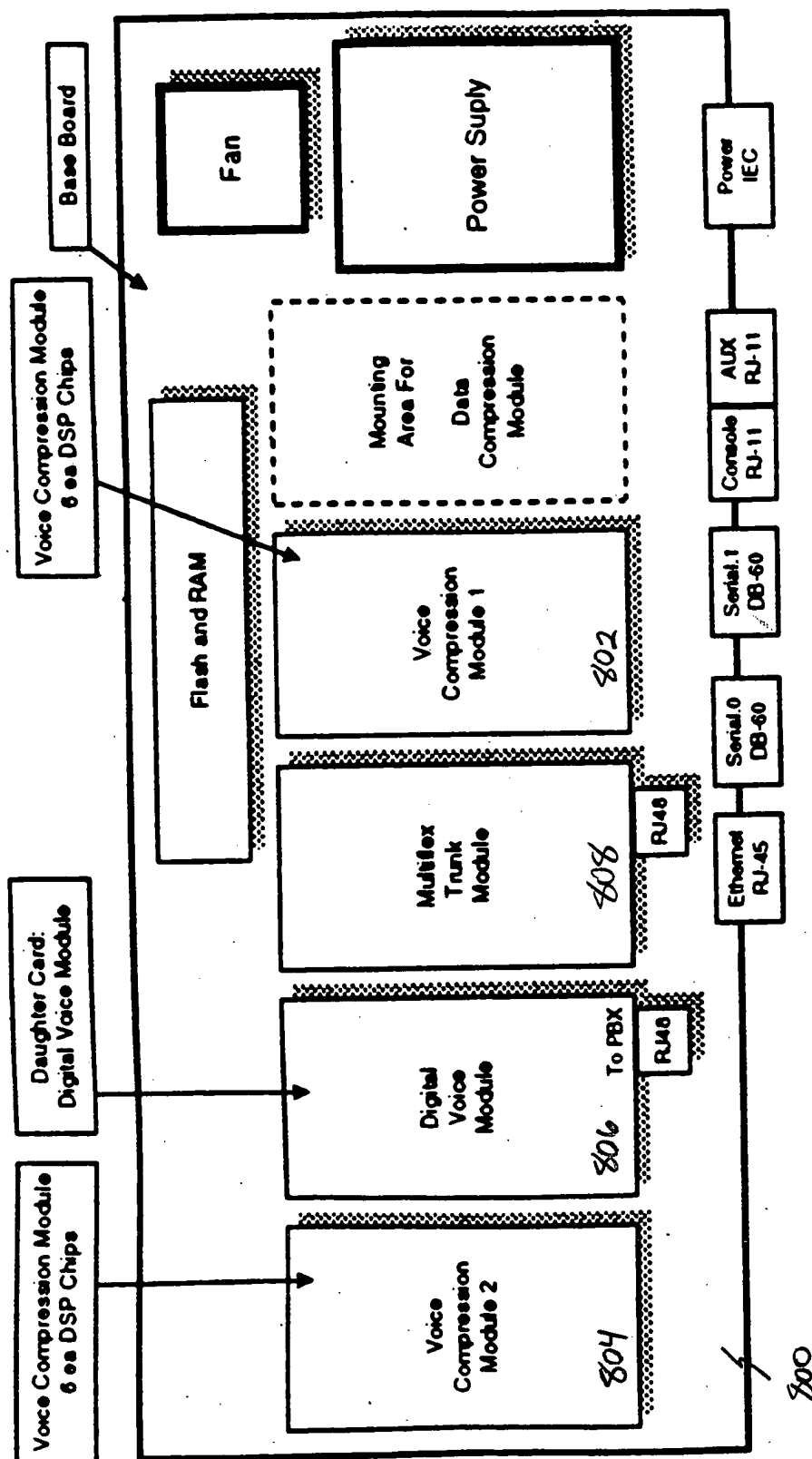


FIGURE 8



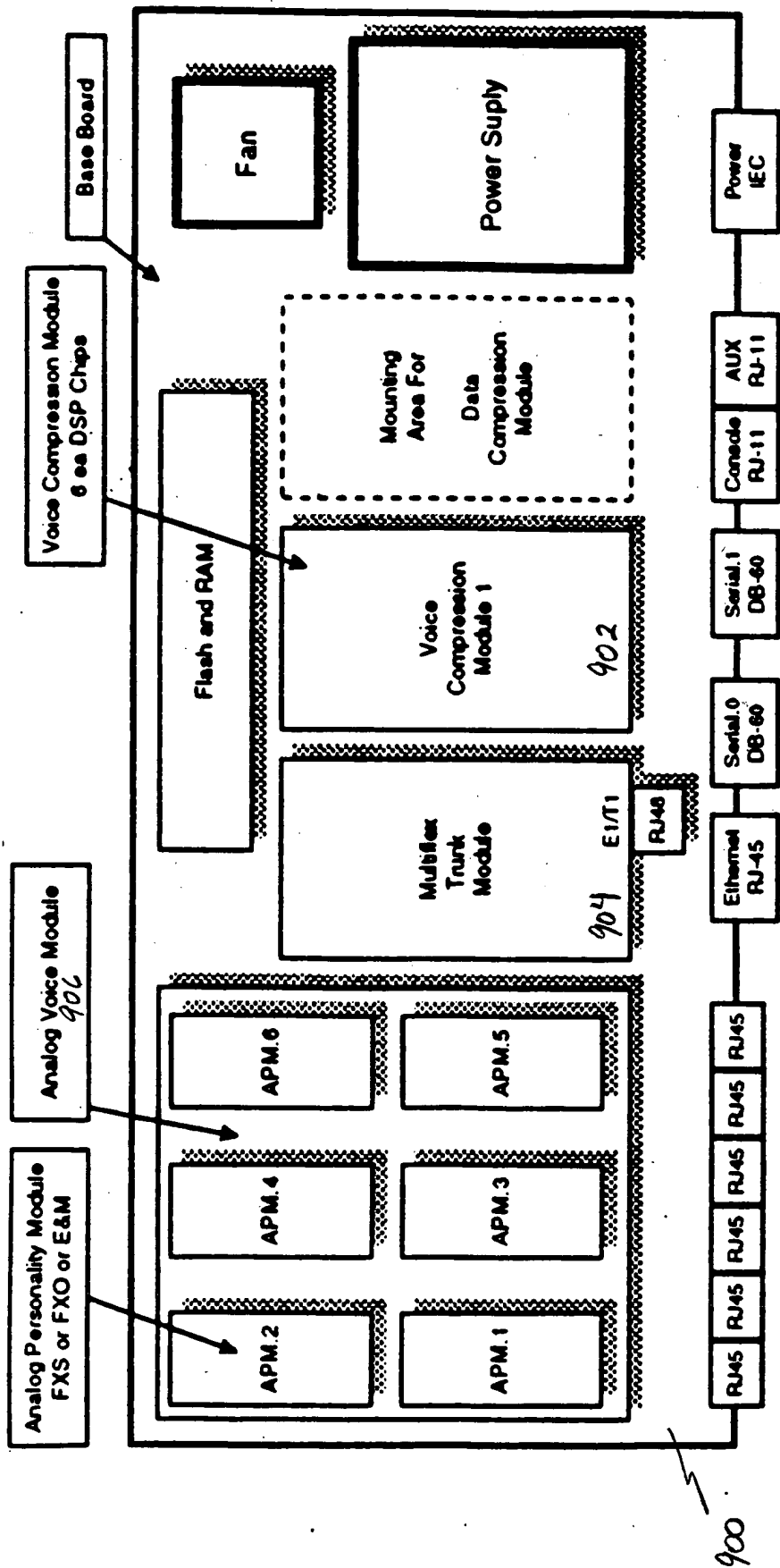


Figure 9

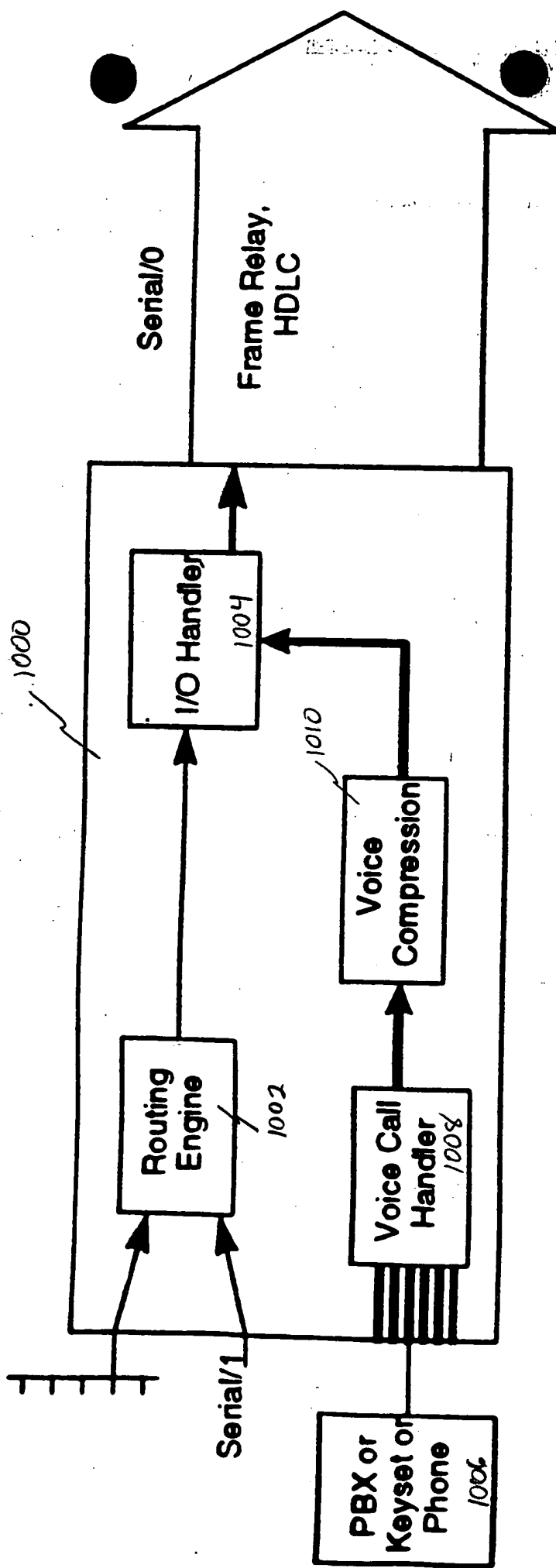


FIGURE 10

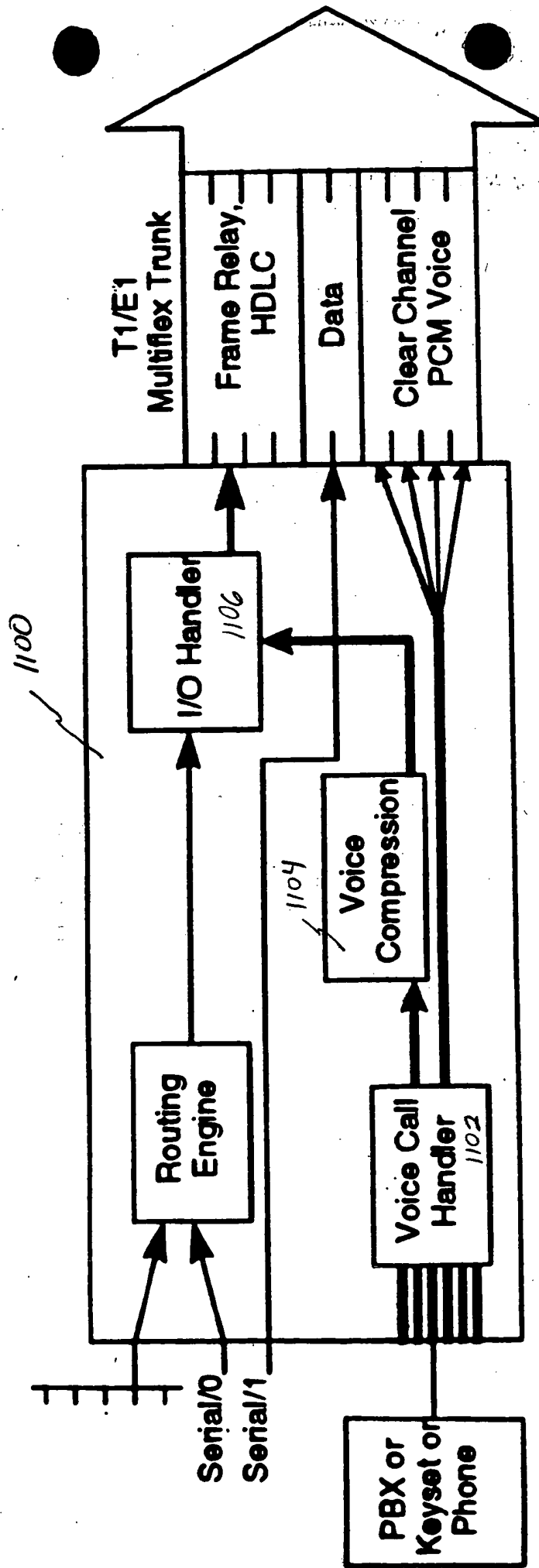


FIGURE 11

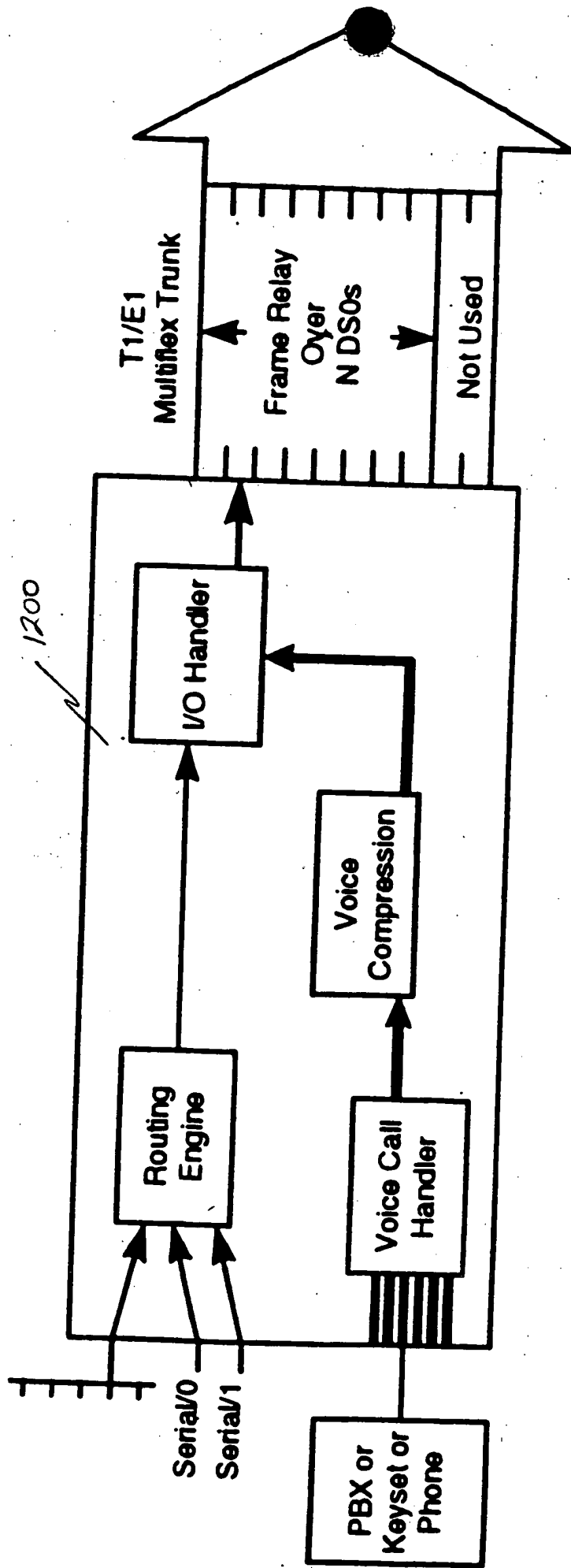


FIGURE 12

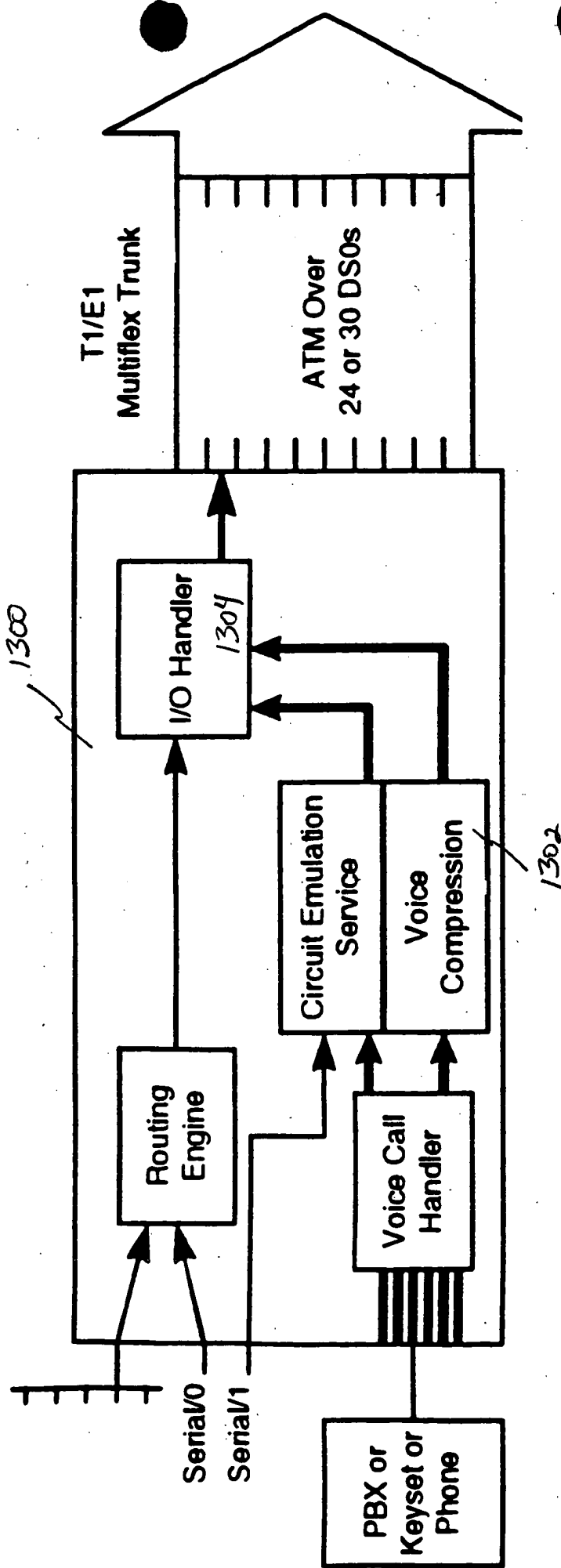


FIGURE 13

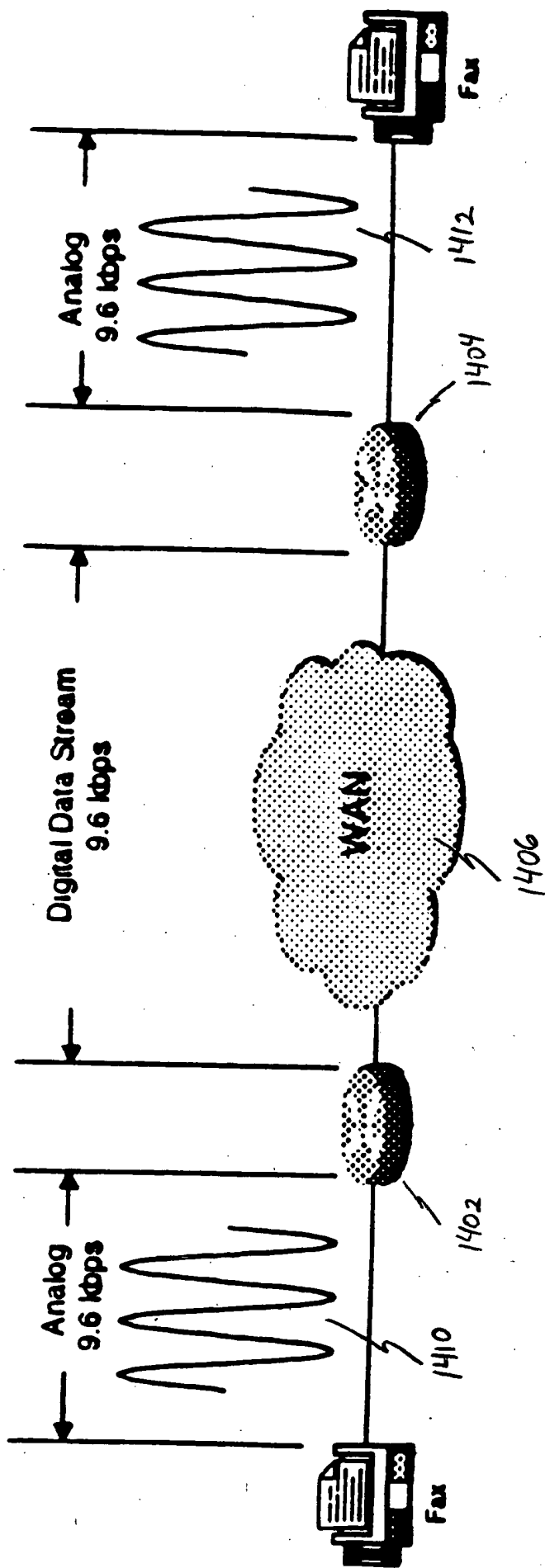


FIGURE 14

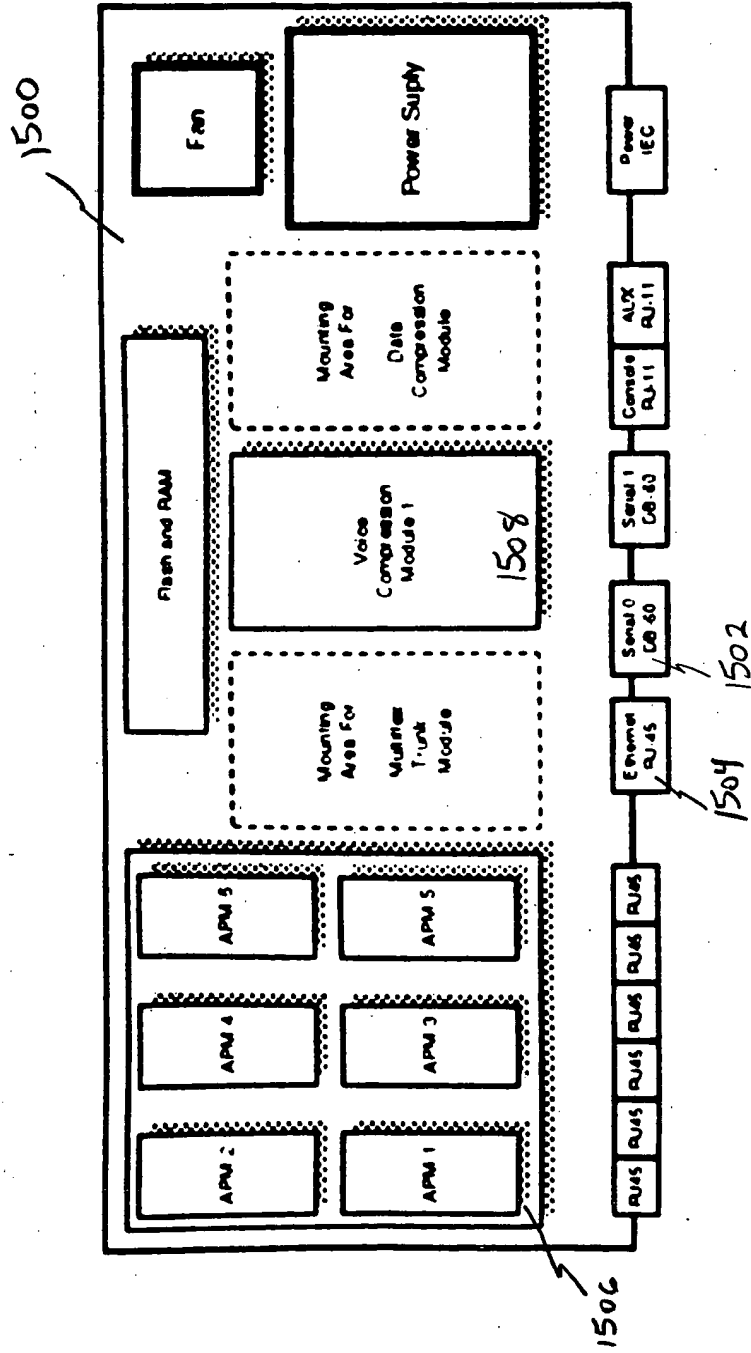


FIGURE 15

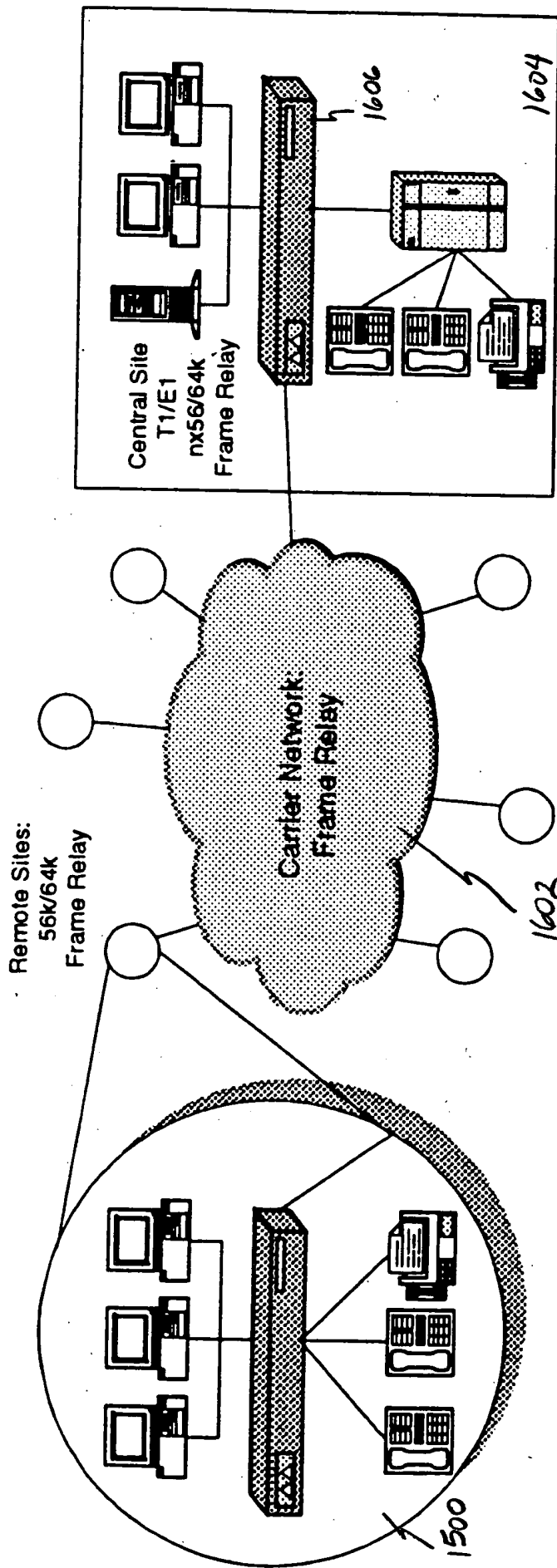


FIGURE 16



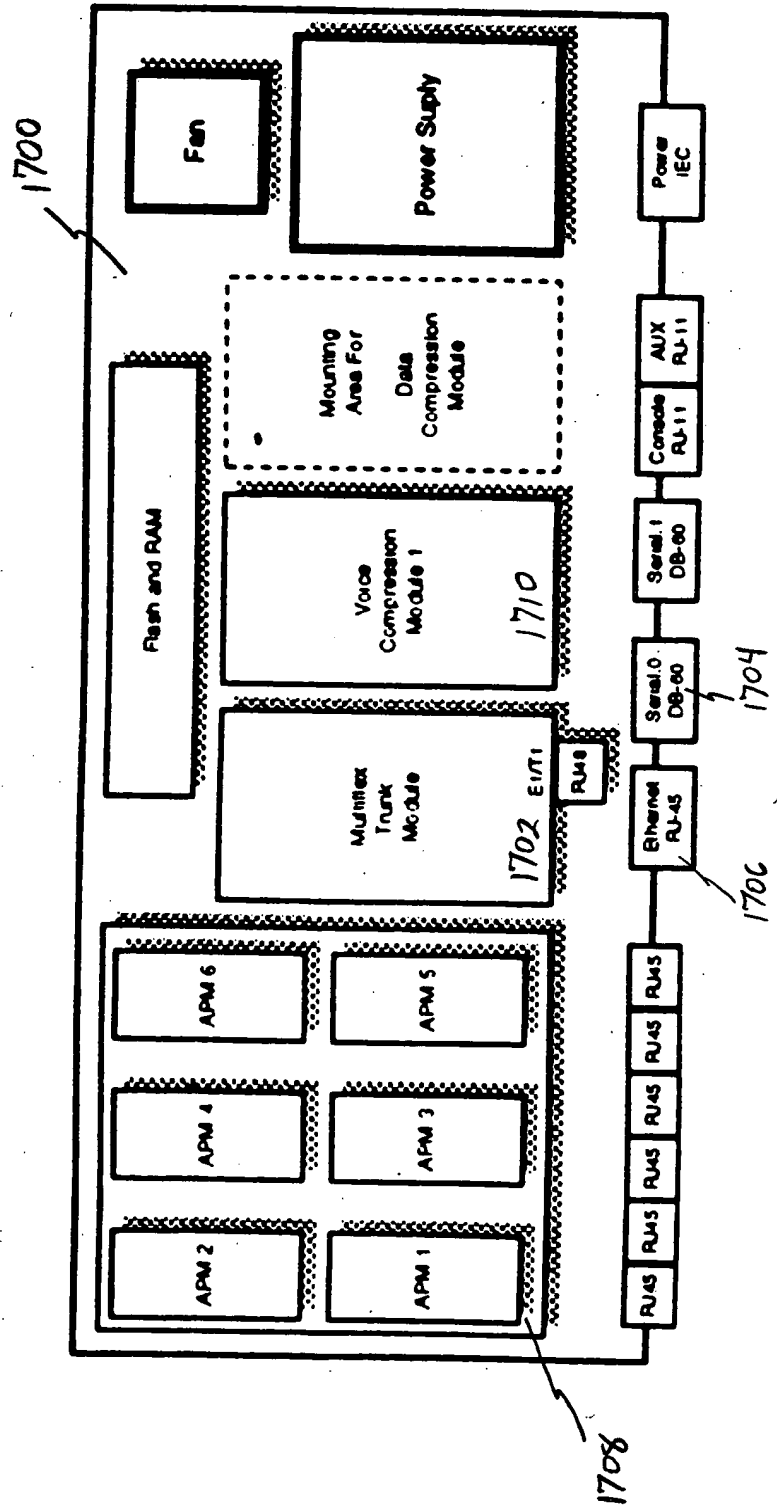


FIGURE 17

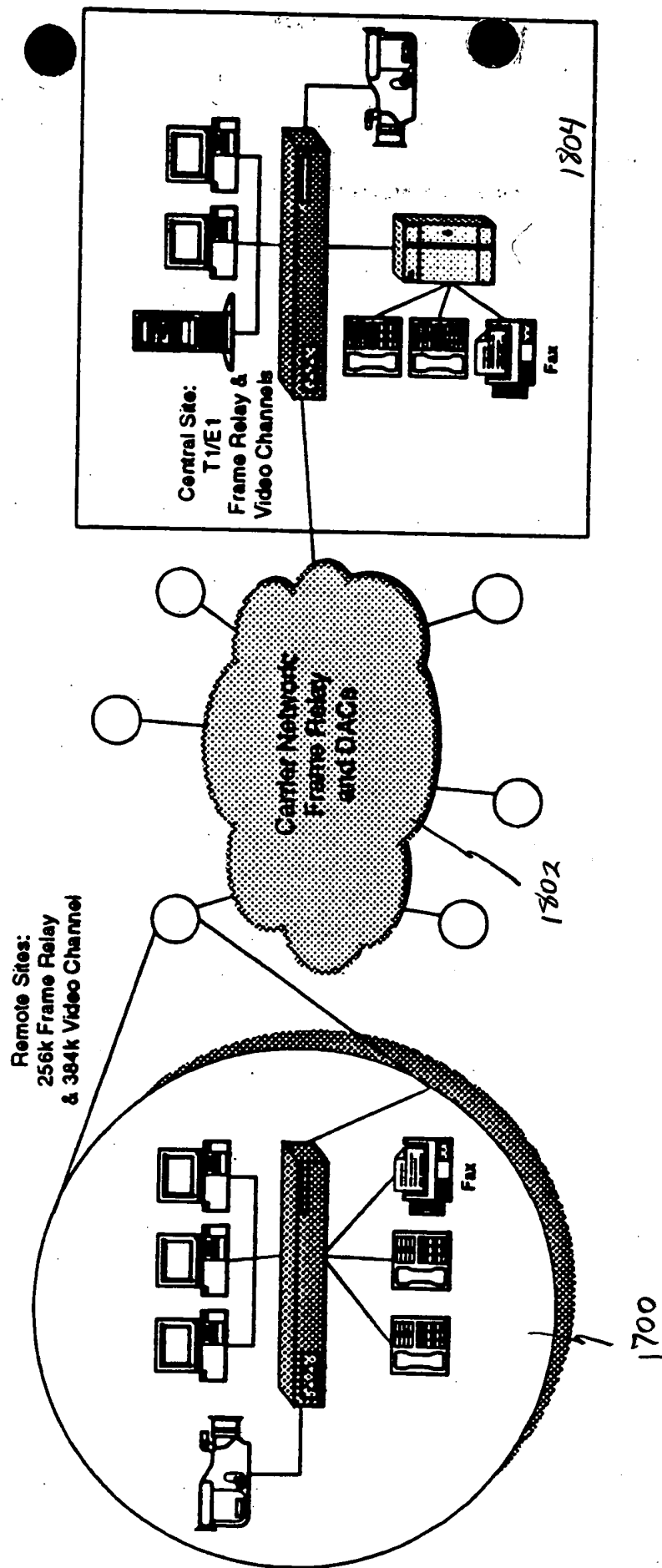


Figure 18

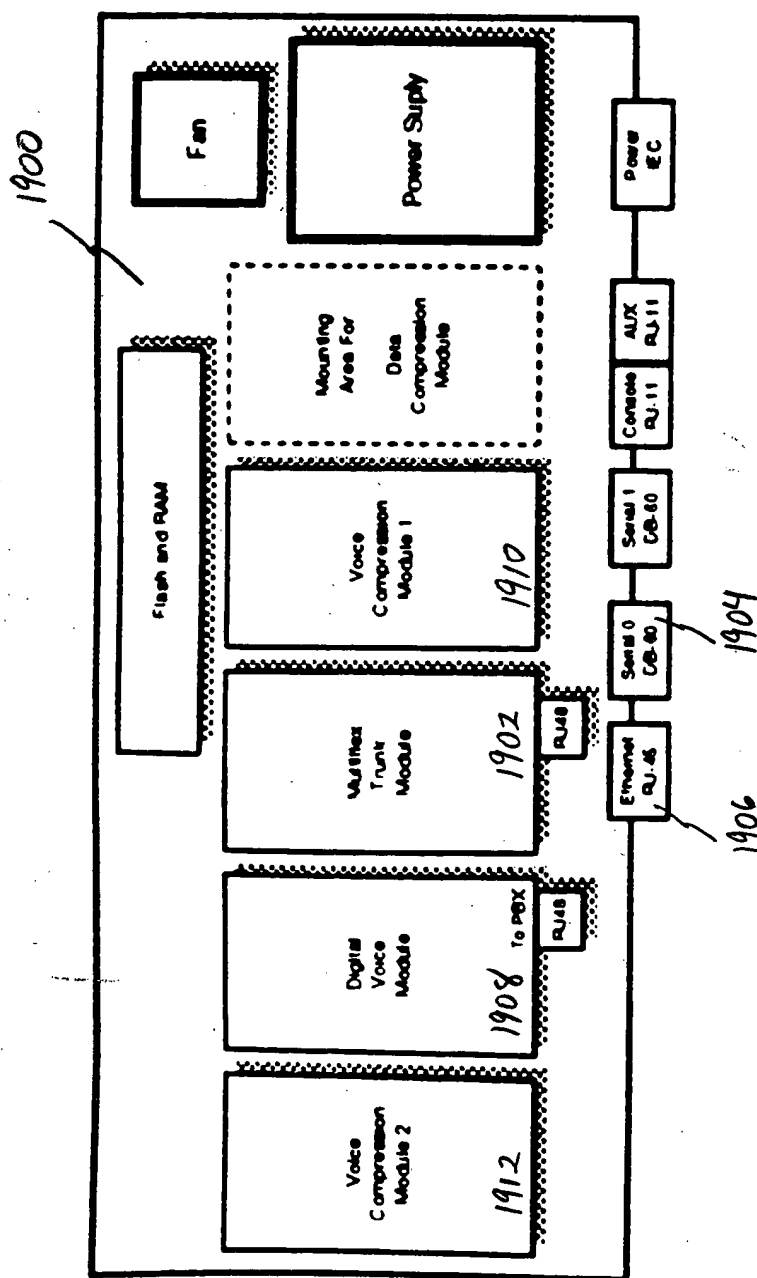


FIGURE 19

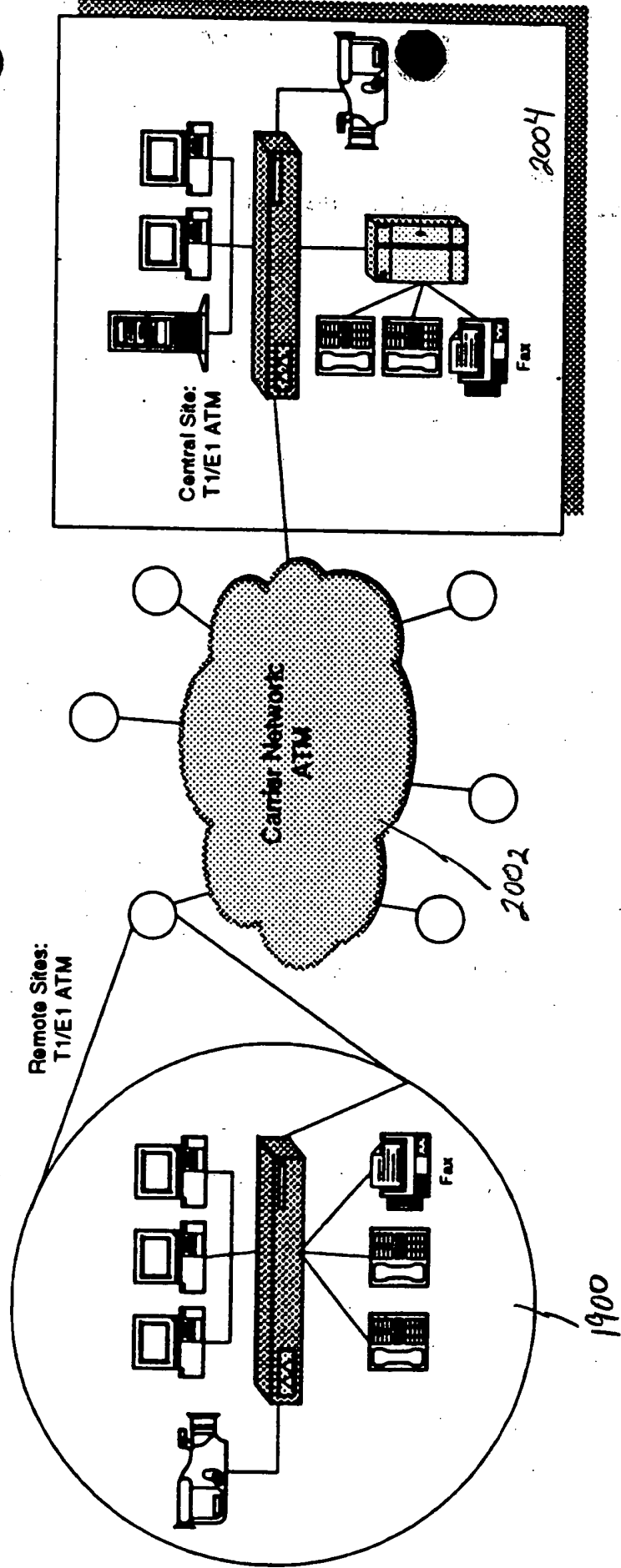


FIGURE 20

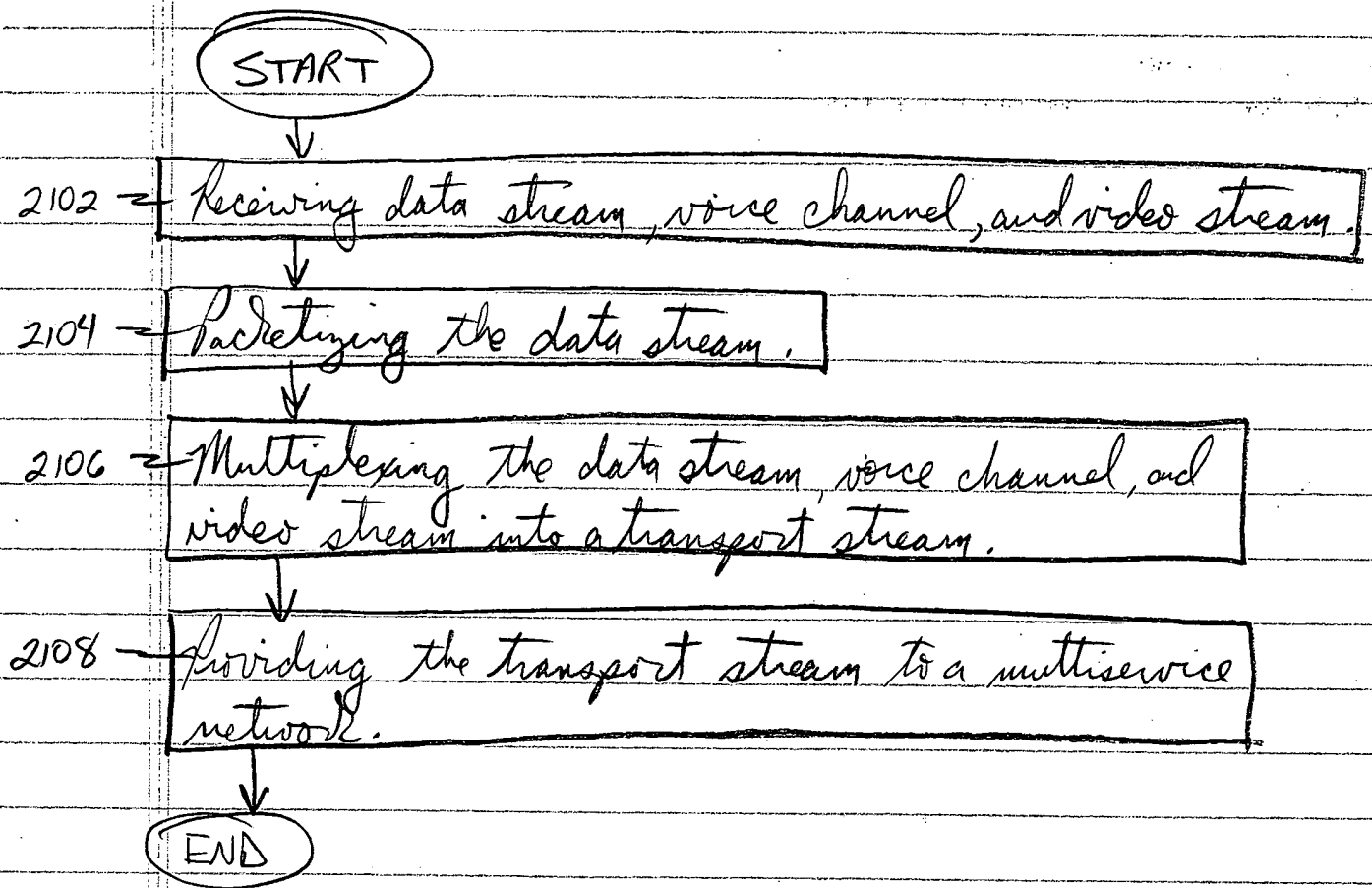


FIGURE 21

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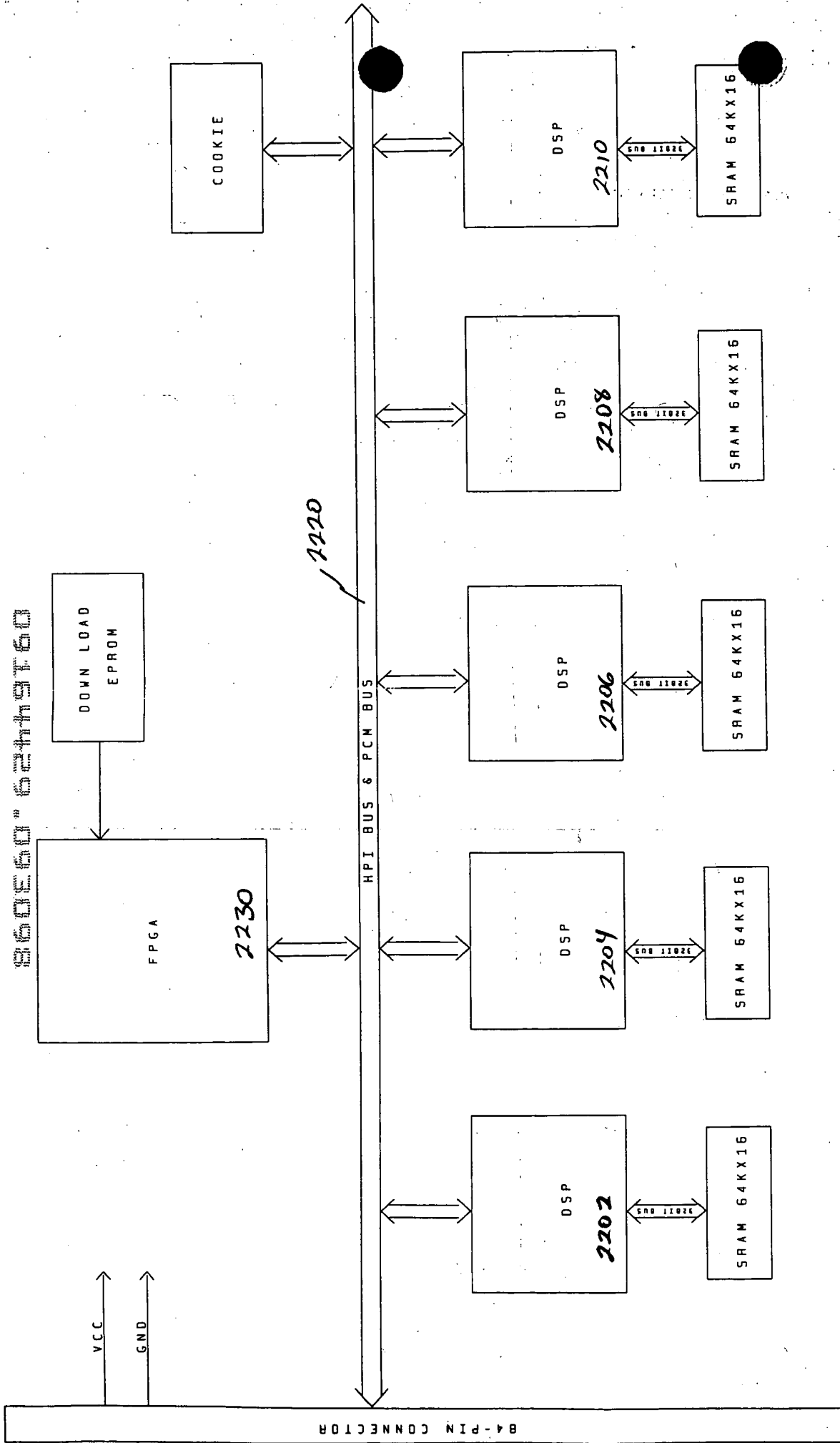


Figure 22

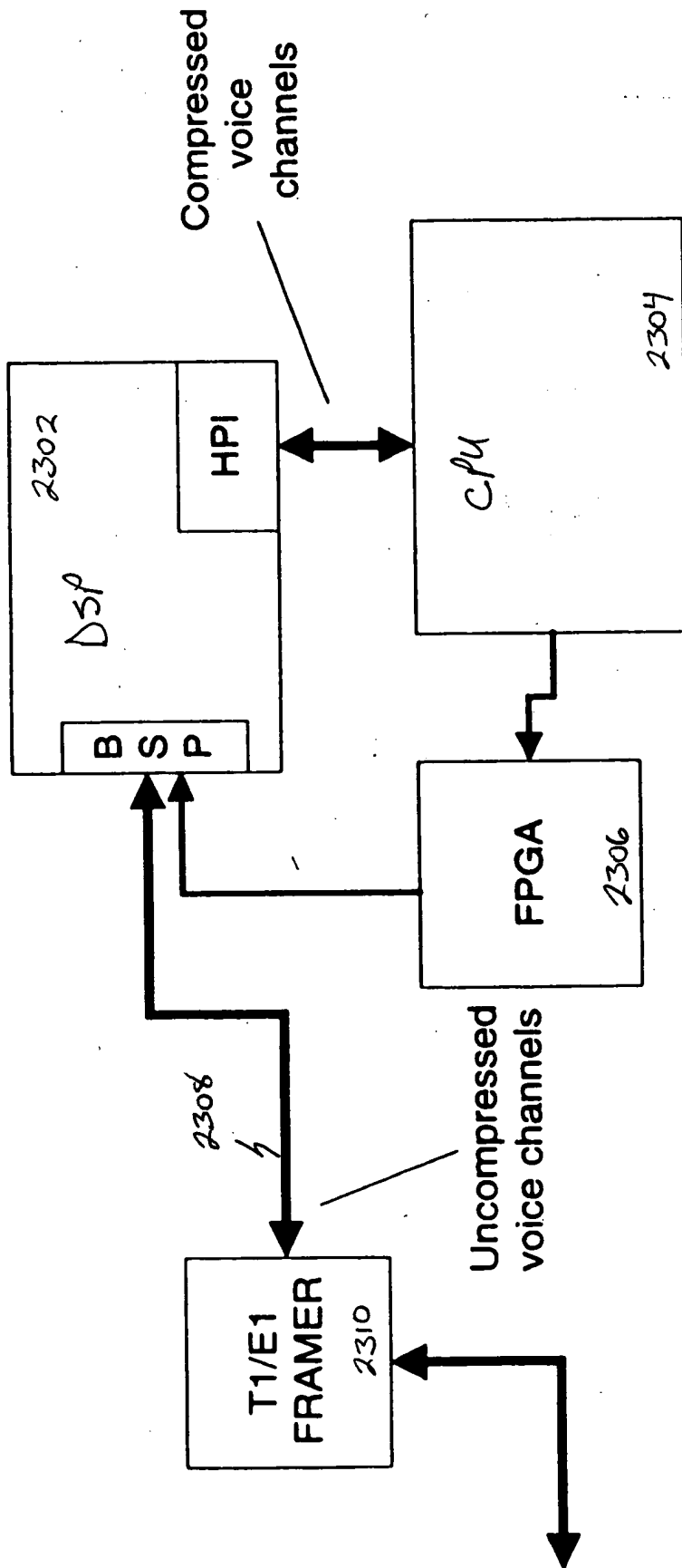


FIGURE 23

The diagram illustrates the hardware architecture with the following components and connections:

- DSP (2402):**
  - Inputs: BDR, BDX, INT3-, BCLKR, BCLKX, BFSR, BFSX.
  - Outputs: HD0-HD7, HBIL, HCNTL0, HCNTL1, HRW-, HCS-, HDS1-, HDS2-, HINT-, HAS-, HPIENA, INT2-.
  - Internal signal: Vdd.
- CPU (2404):**
  - Inputs: D0-D7, A31, A30, A29, RW-, CS-, WE0-, IRQ-.
  - Outputs: PCLK, WE-, CSx, ADDR., D0-D4.
- FPGA (2406):**
  - Inputs: 2.048 MHz CLK, FS-.
  - Outputs: FSCx, GRCLKx.

**Connections:**

- The CPU's D0-D7 bus is connected to the DSP's HD0-HD7 bus.
- The CPU's A31, A30, and A29 address lines are connected to the DSP's HBIL, HCNTL0, and HCNTL1 control lines, respectively.
- The CPU's RW- control line is connected to the DSP's HRW- control line.
- The CPU's CS- control line is connected to the DSP's HCS- control line.
- The CPU's WE0- control line is connected to the DSP's HDS1- control line.
- The CPU's IRQ- input is connected to the DSP's HINT- control line.
- The CPU's PCLK output is connected to the DSP's BCLKR input.
- The CPU's WE- output is connected to the DSP's BCLKX input.
- The CPU's CSx output is connected to the DSP's BFSR input.
- The CPU's ADDR. output is connected to the DSP's BFSX input.
- The CPU's D0-D4 output is connected to the DSP's INT3- input.
- The FPGA's 2.048 MHz CLK output is connected to the DSP's BCLKX input.
- The FPGA's FS- output is connected to the DSP's BFSX input.
- The FPGA's FSCx output is connected to the DSP's HDS2- control line.
- The FPGA's GRCLKx output is connected to the DSP's HPIENA control line.

FIGURE 24



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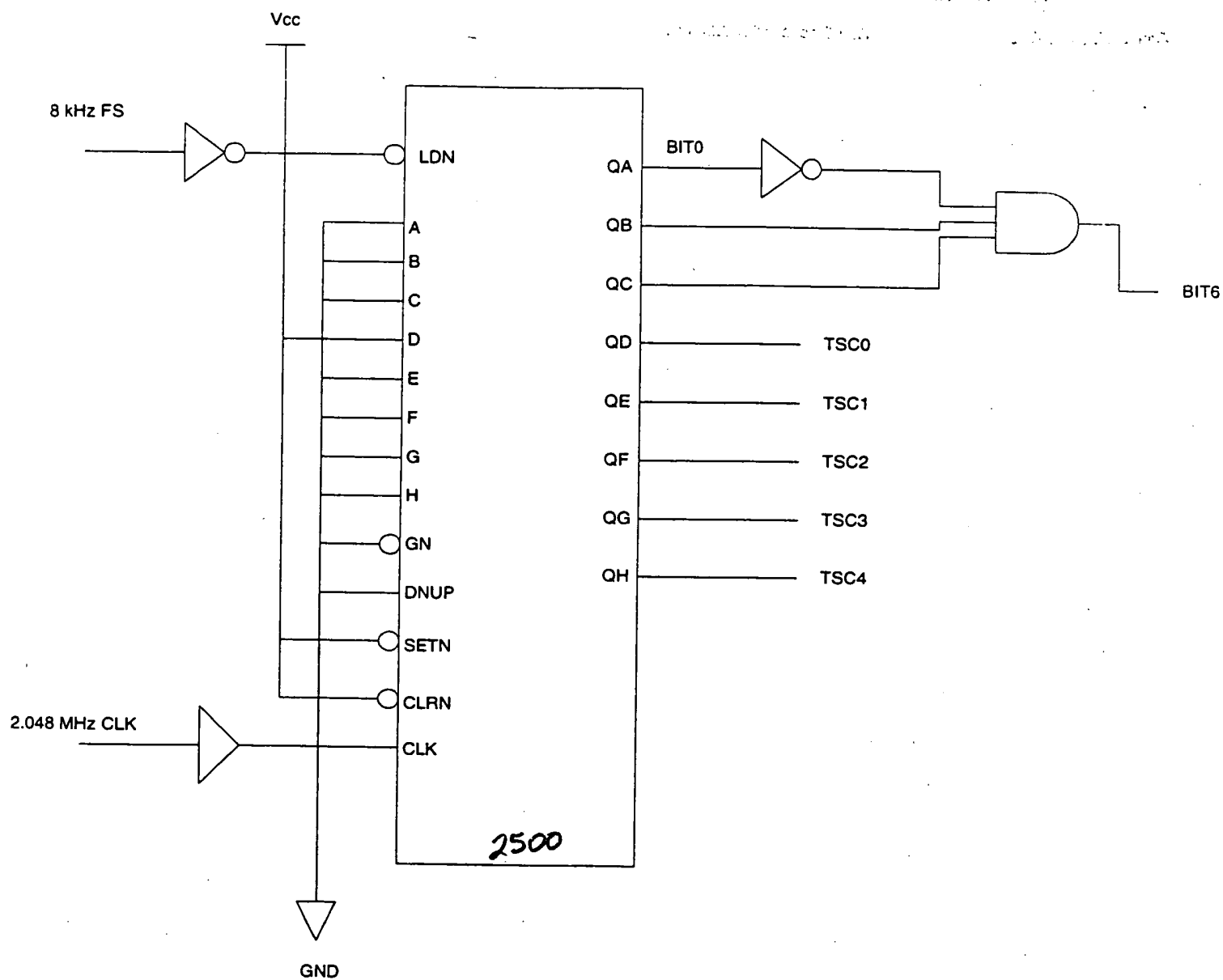


FIGURE 25

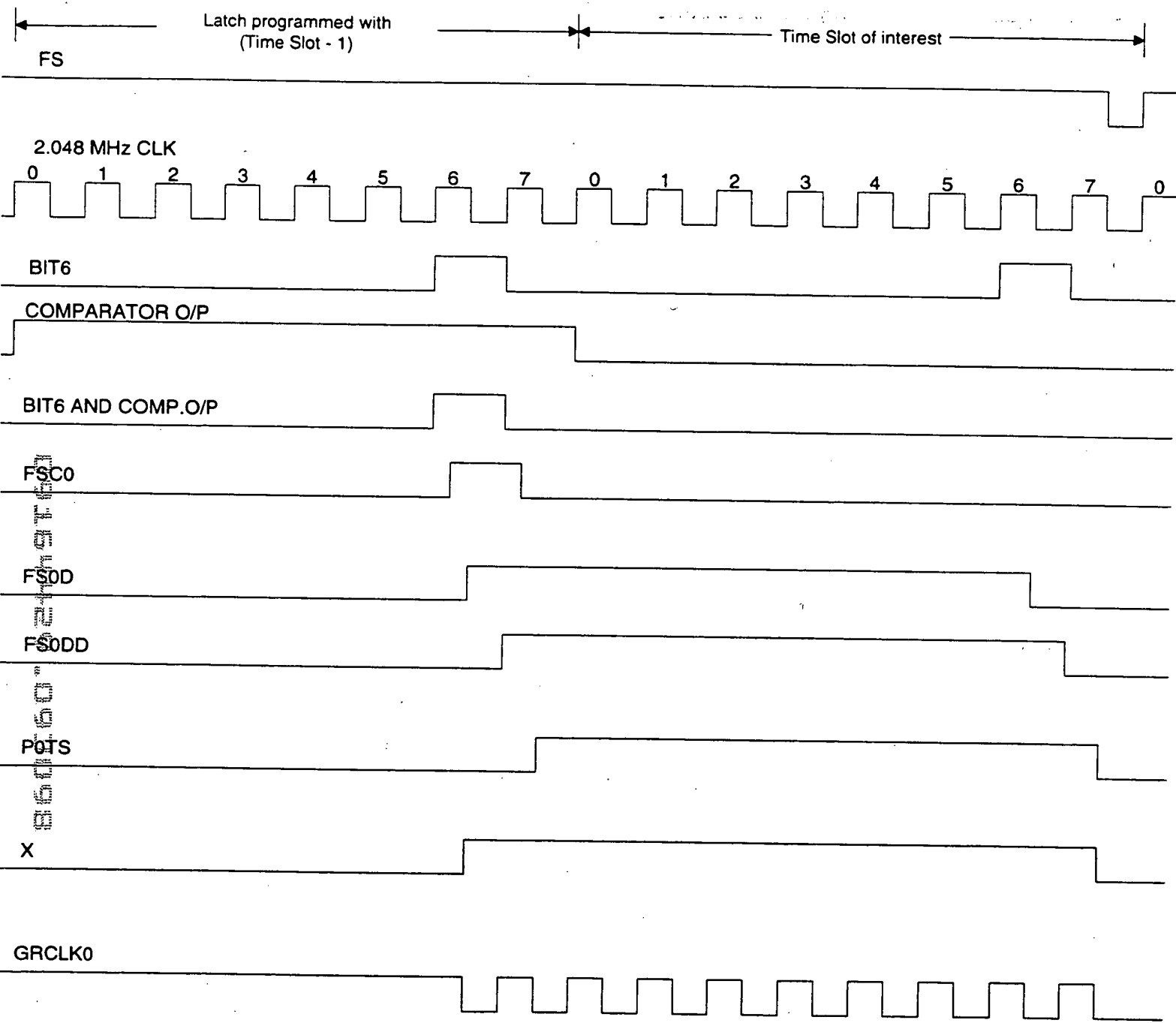


FIGURE 26

860E60-62449160

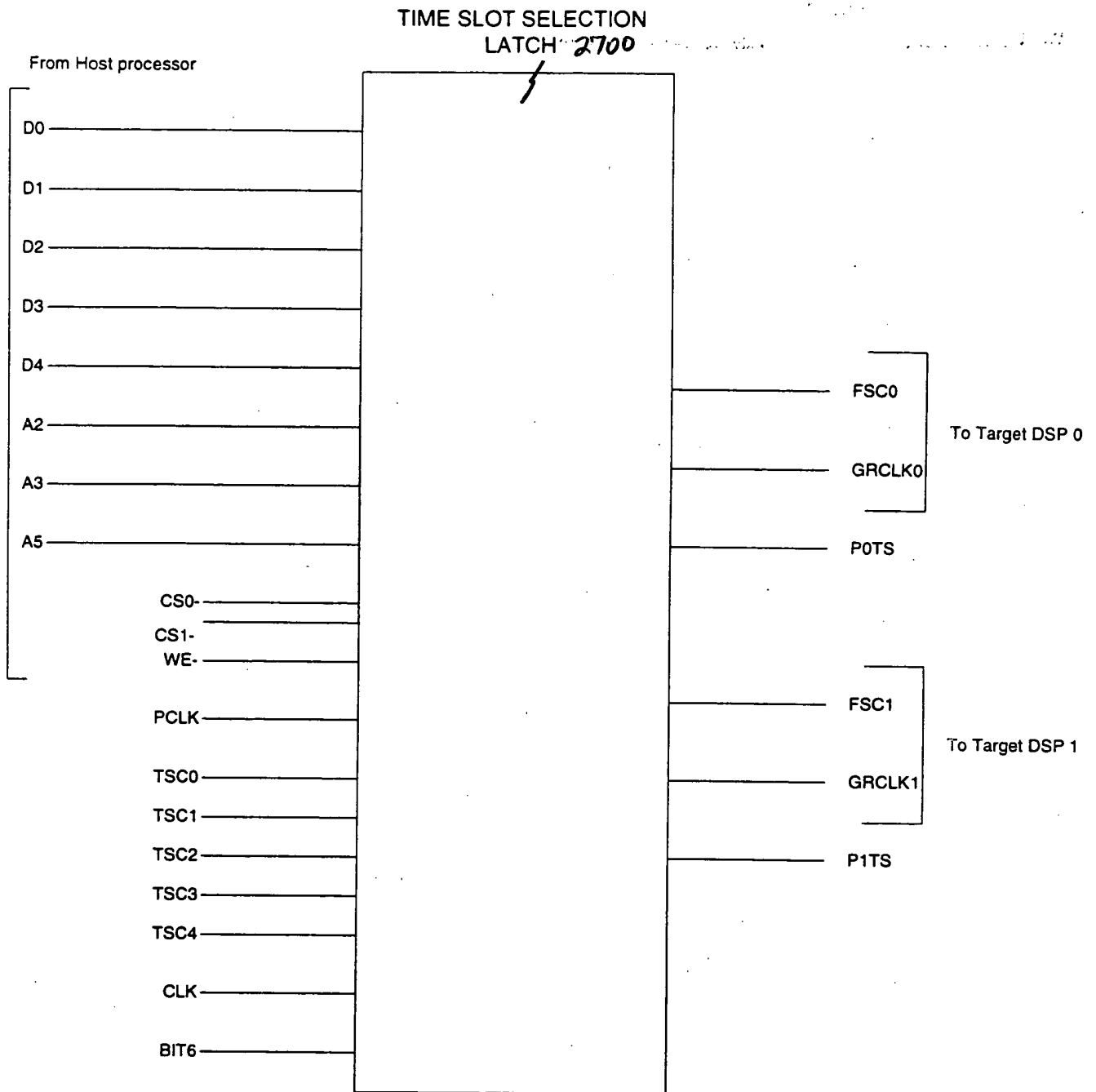


FIGURE 27

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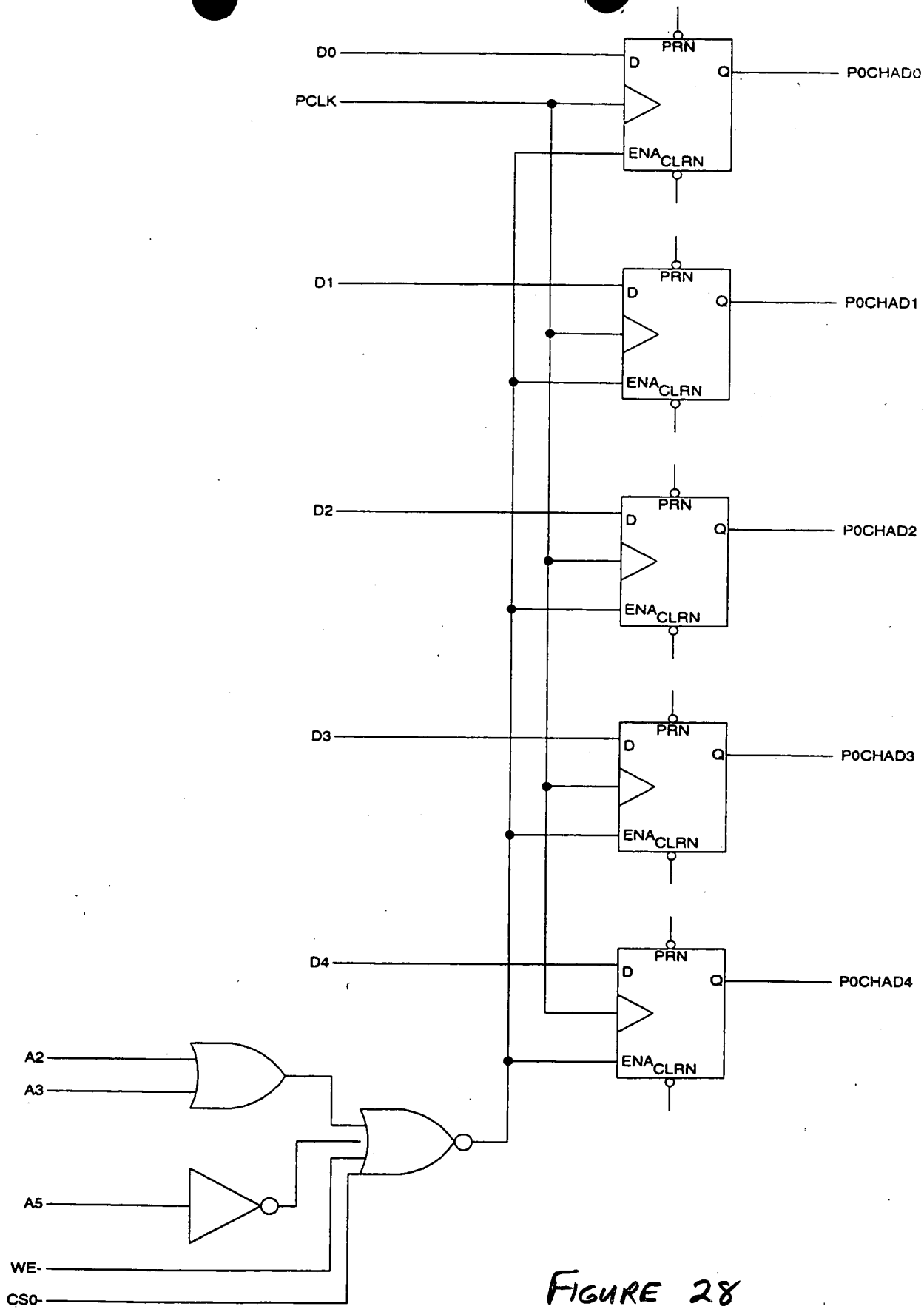


FIGURE 28

860E60-62449T60

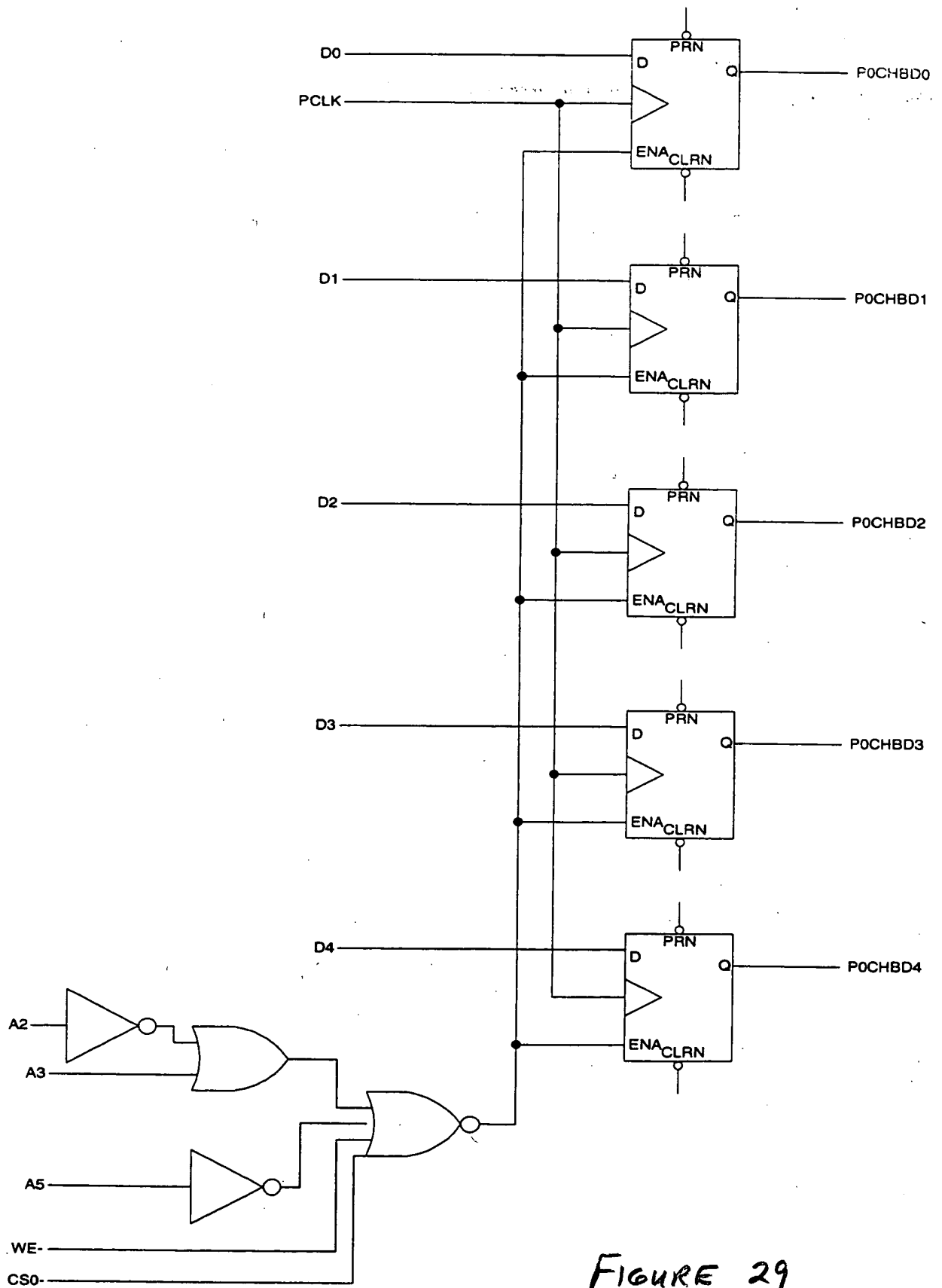


FIGURE 30

860E60" 62449T60

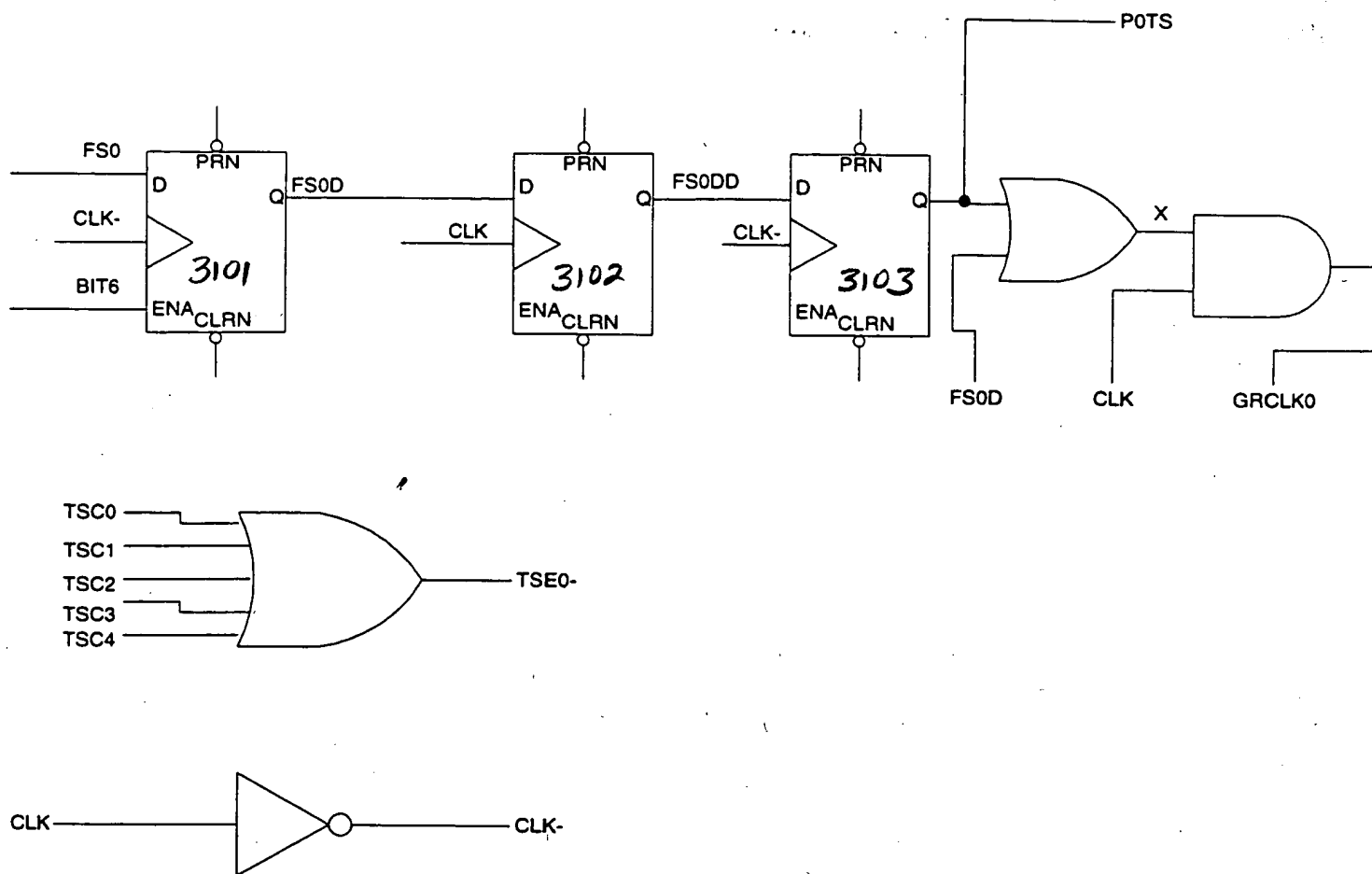


FIGURE 31

860E60"62449160

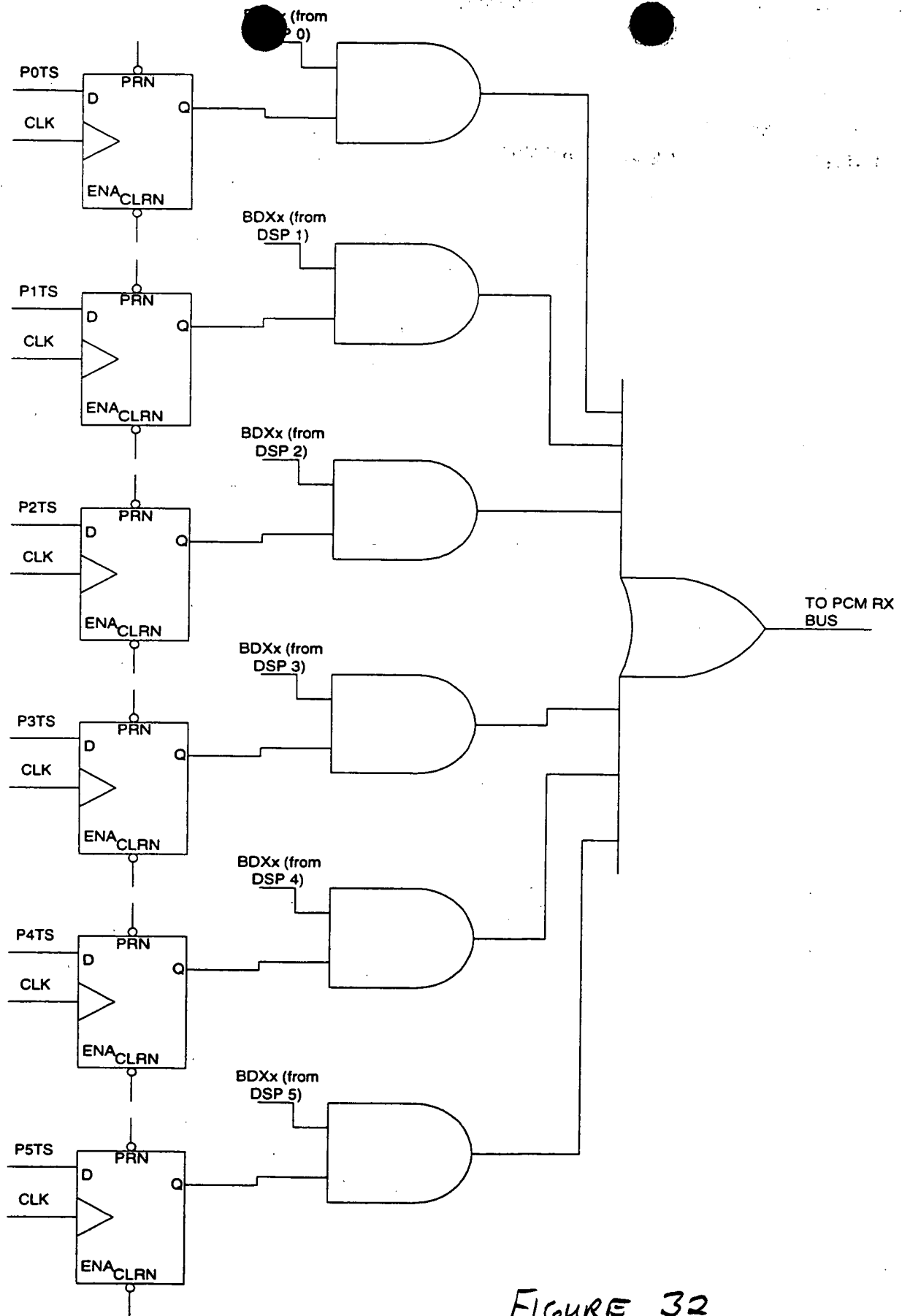


FIGURE 32



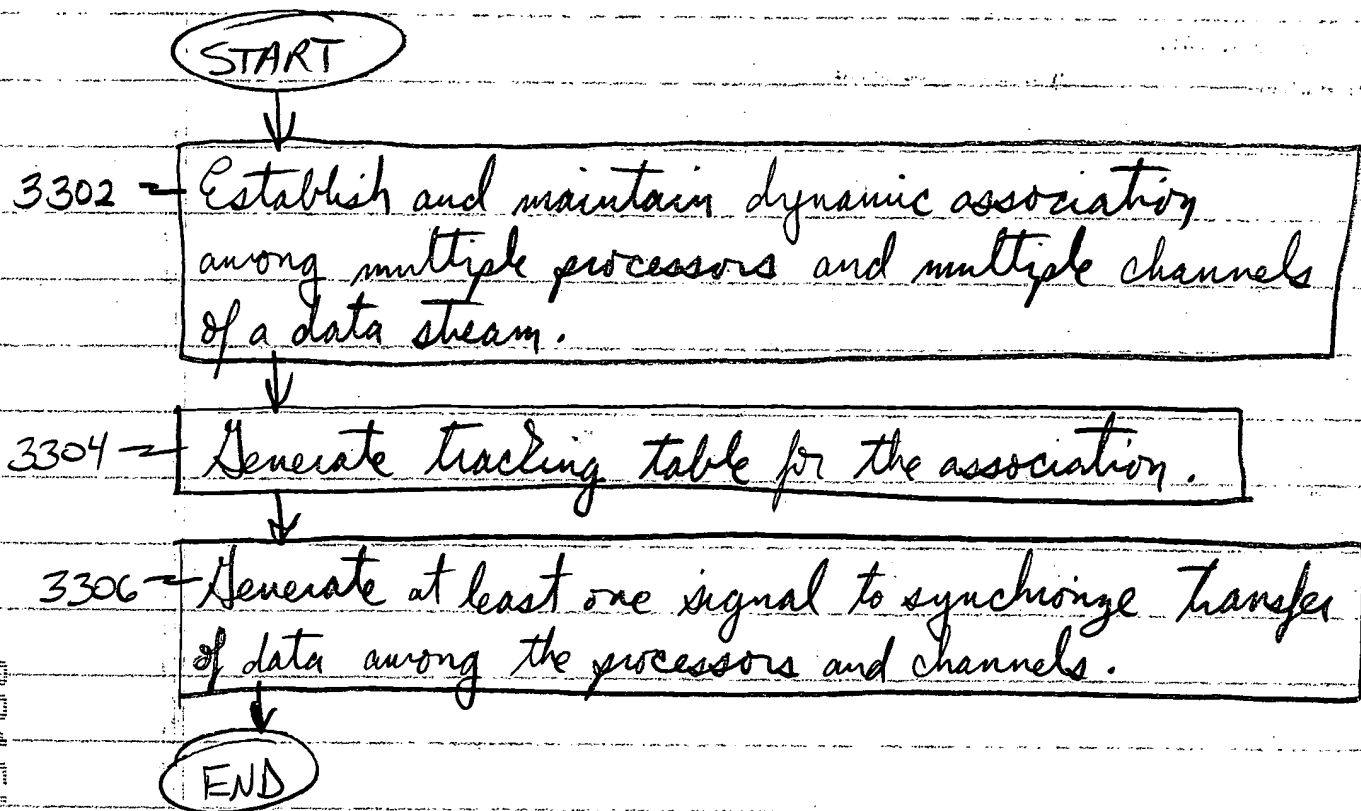


FIGURE 33

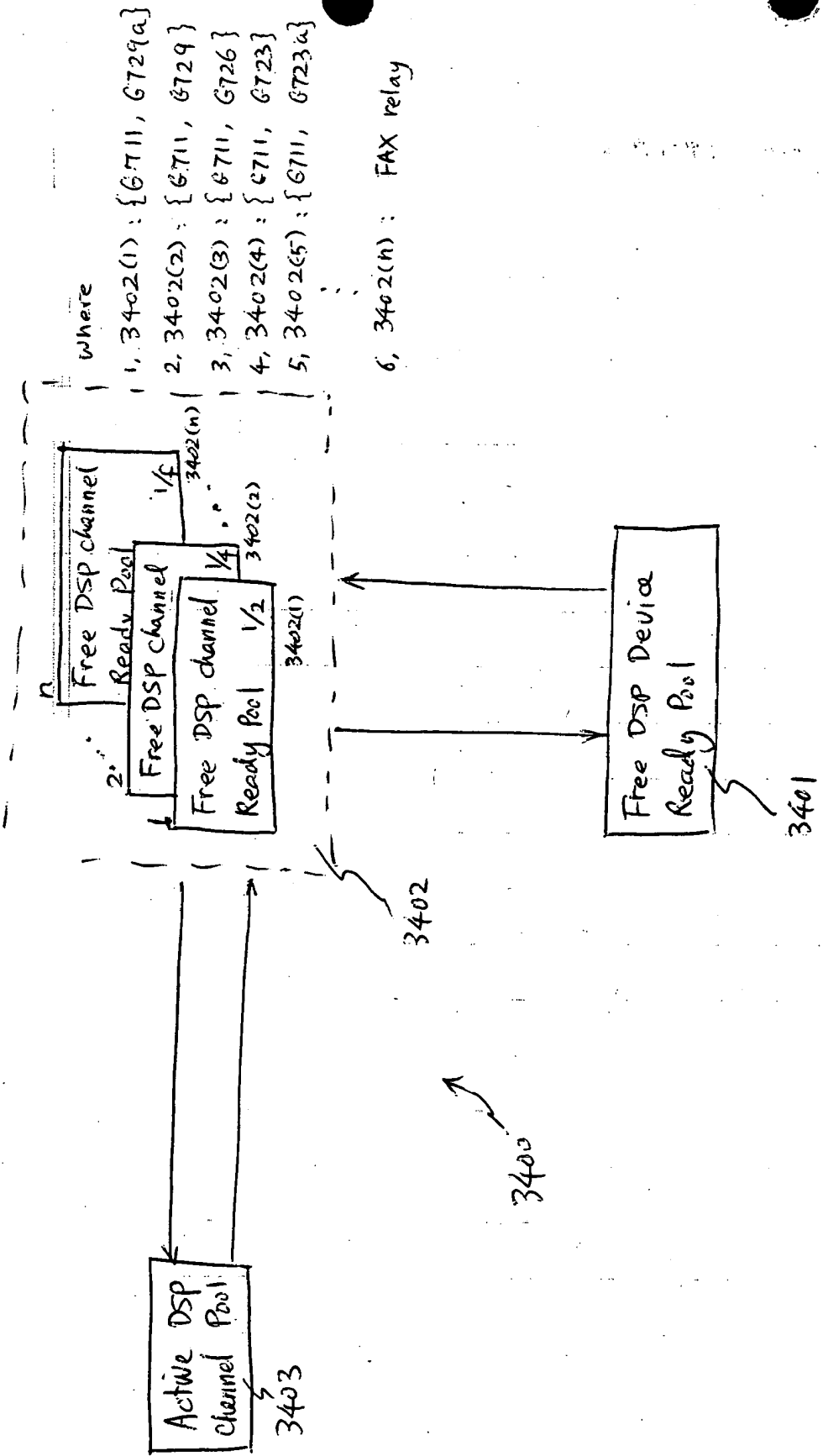


Figure 34

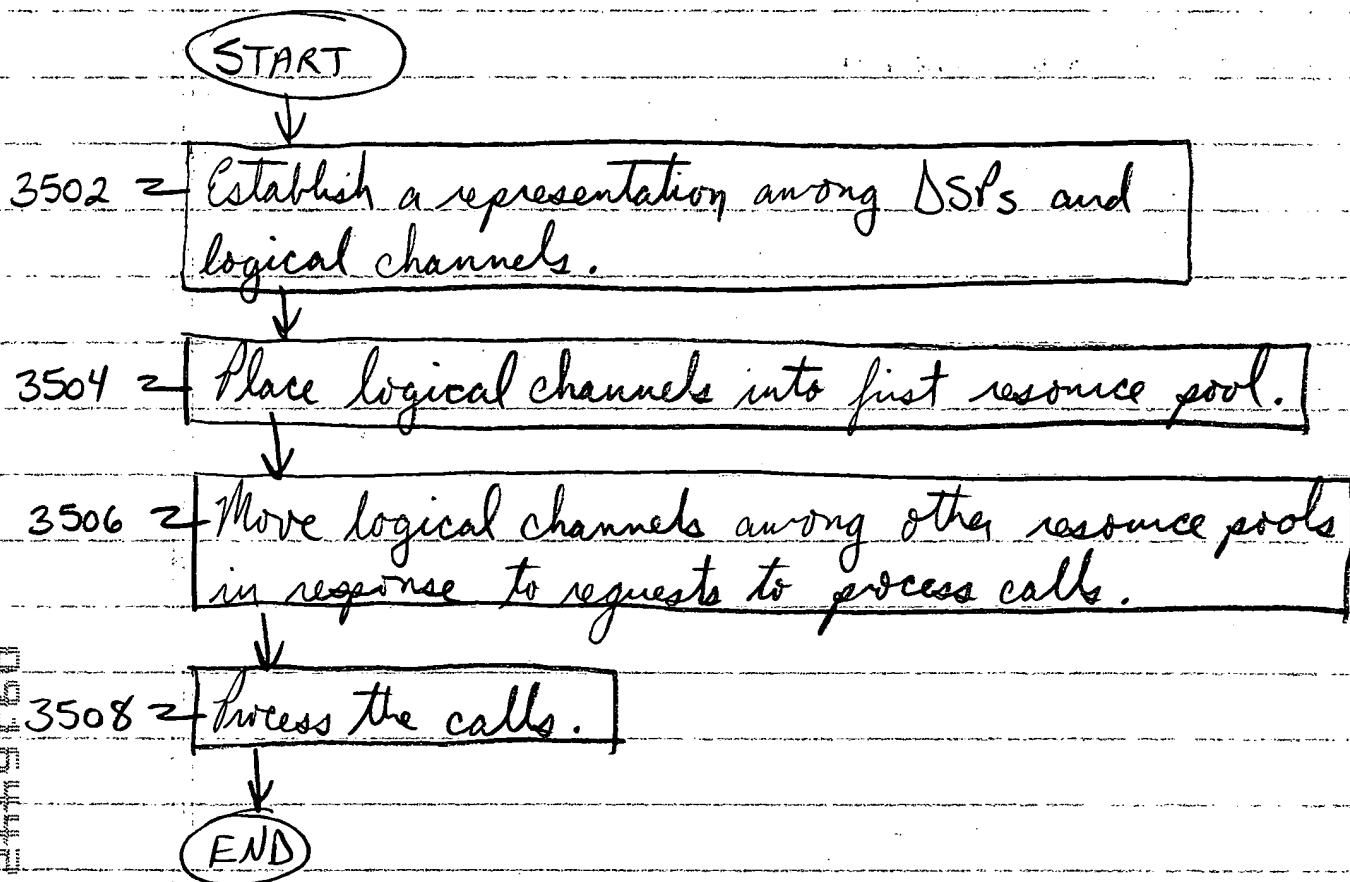


FIGURE 35

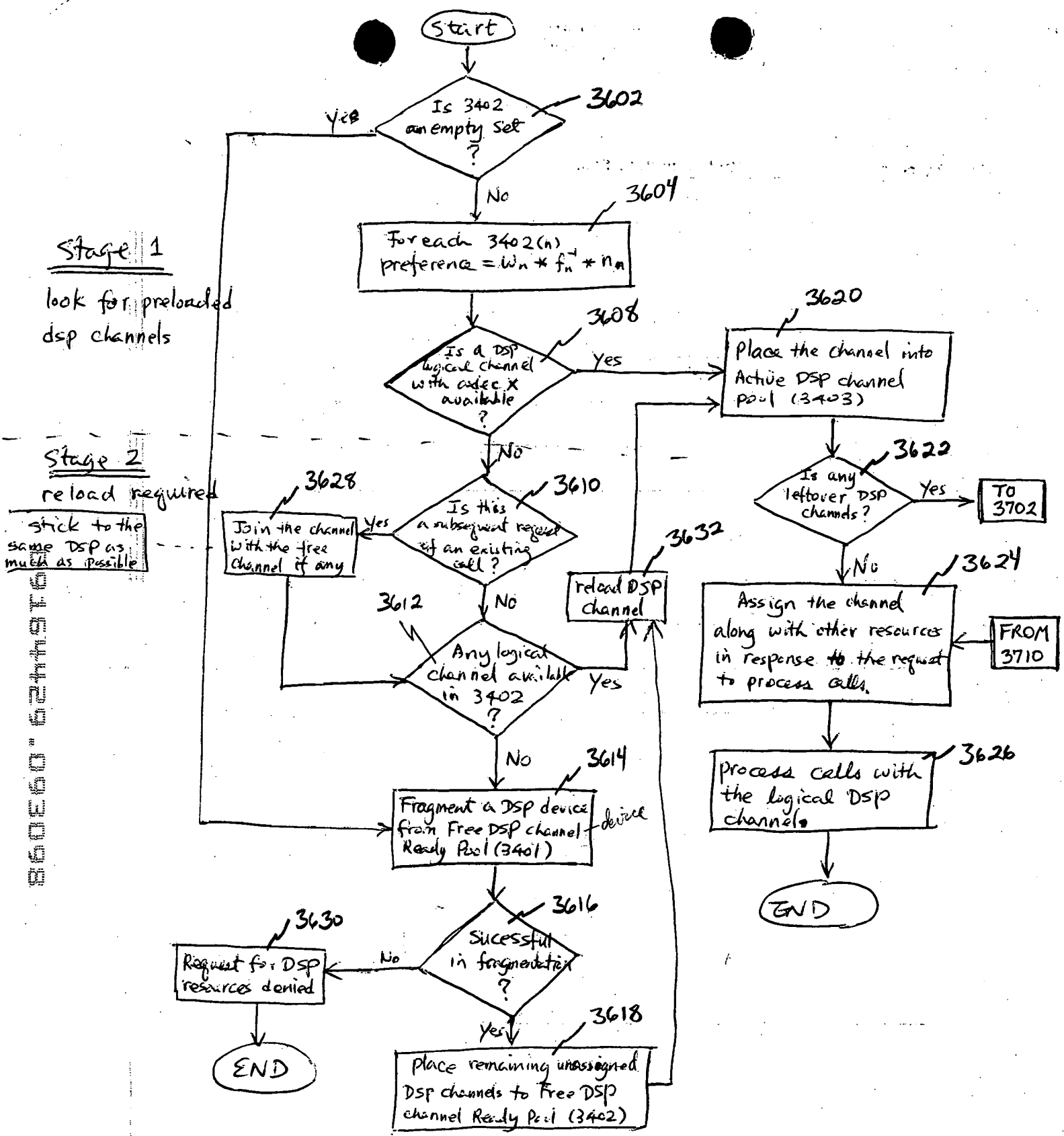


FIGURE 36

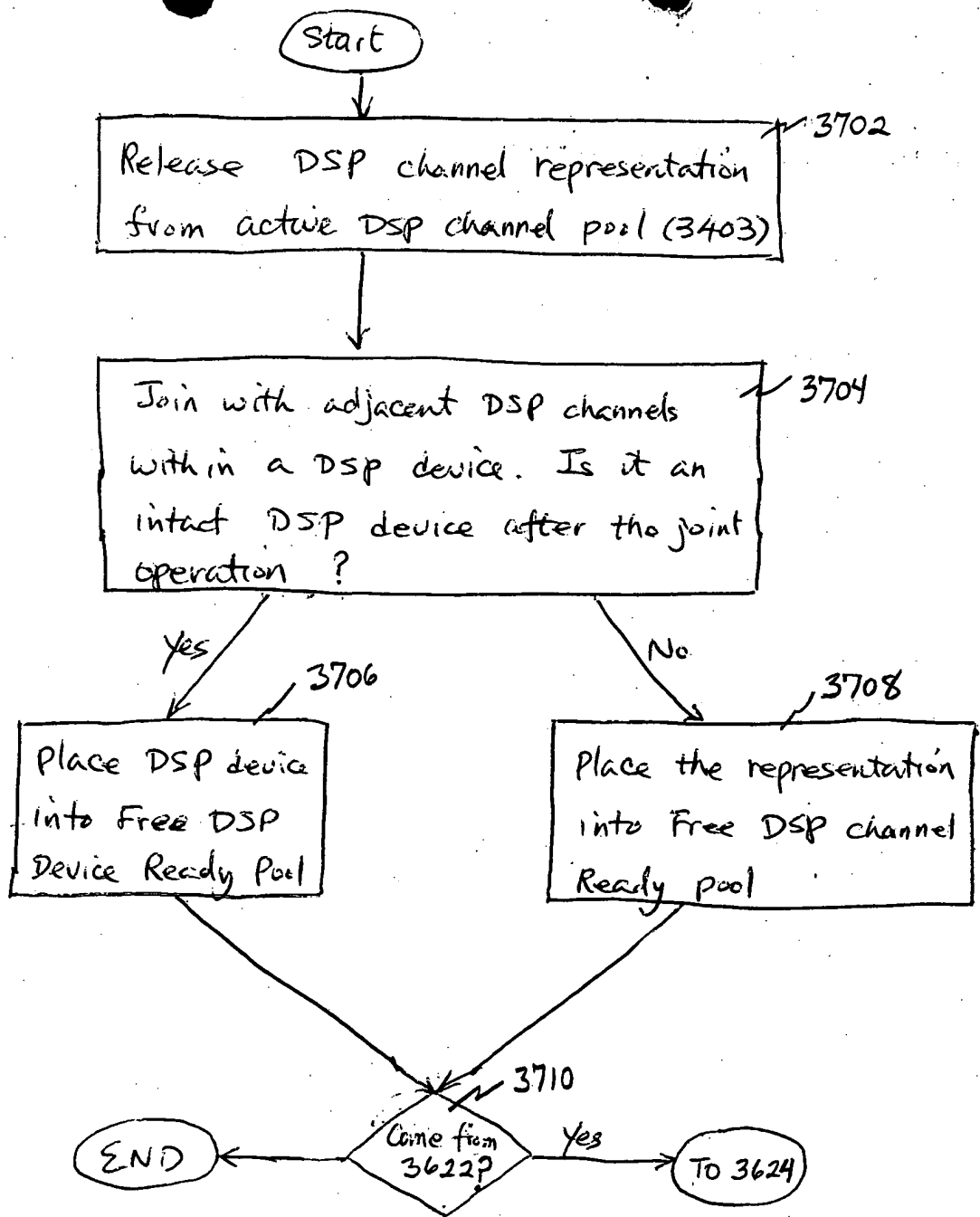


FIGURE 37

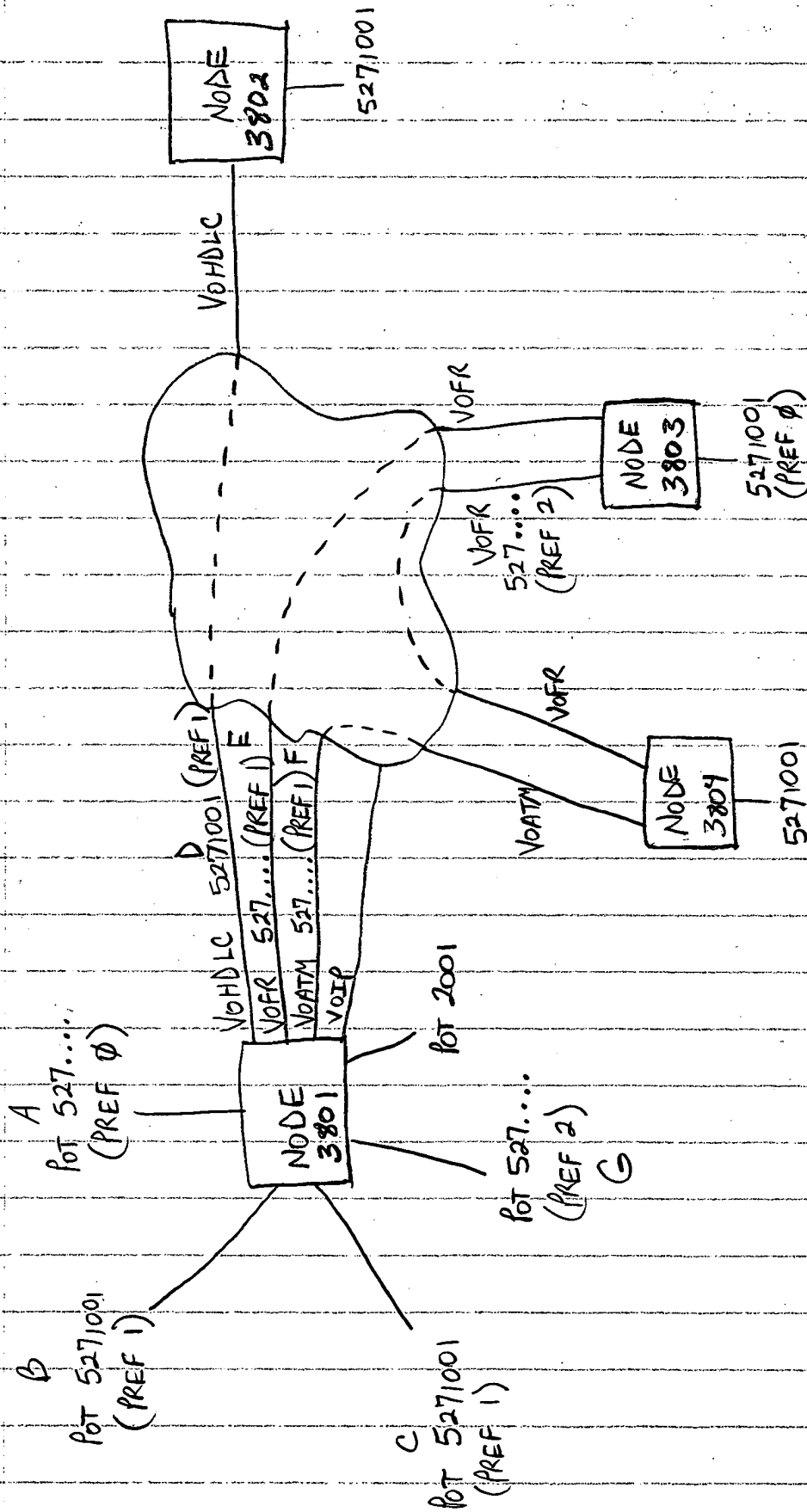


Figure 38

PRIORITY

1	POT 527.... (PREF $\emptyset$ )	A
2	POT 527 1001 (PREF 1)	B
3	POT 527 1001 (PREF 1)	C
4	VOHDL 527 1001 (PREF 1)	D
5	VOFR 527.... (PREF 1)	E
6	VOATM 527.... (PREF 1)	F
7	POT 527.... (PREF 2)	G

FIGURE 39

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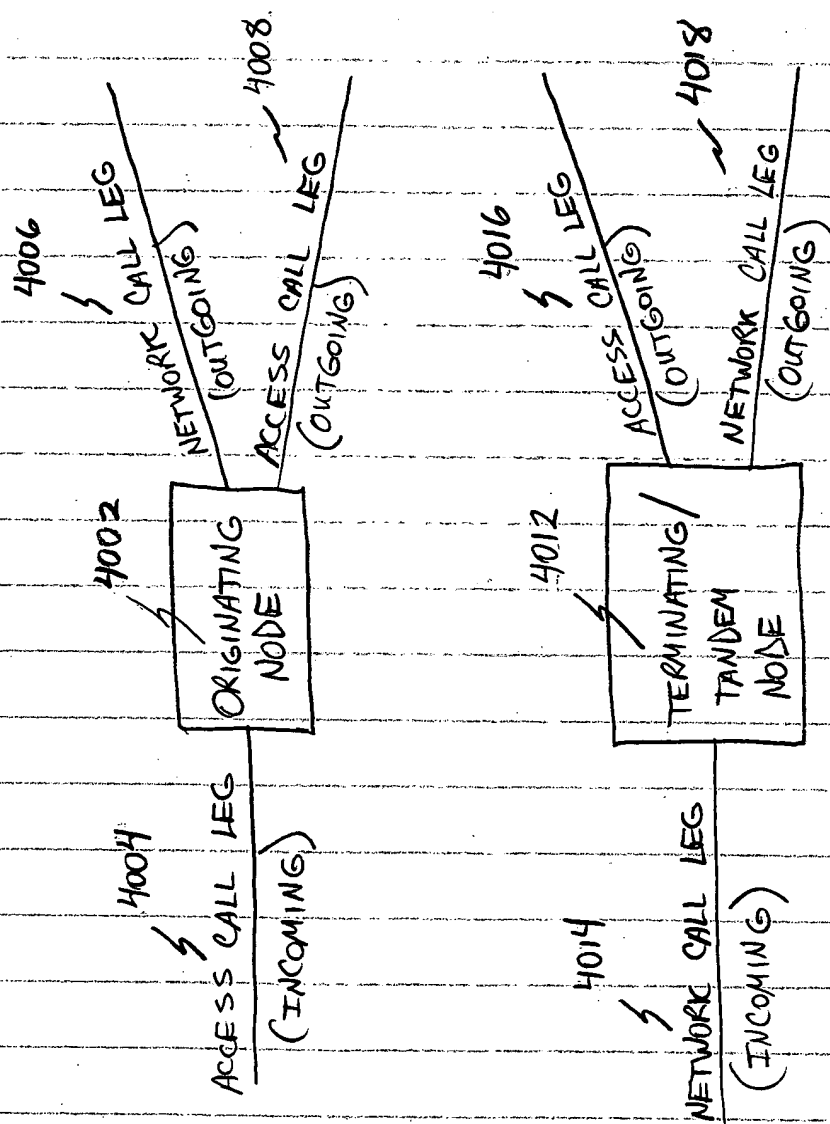


FIGURE 40



860E60 62449T60

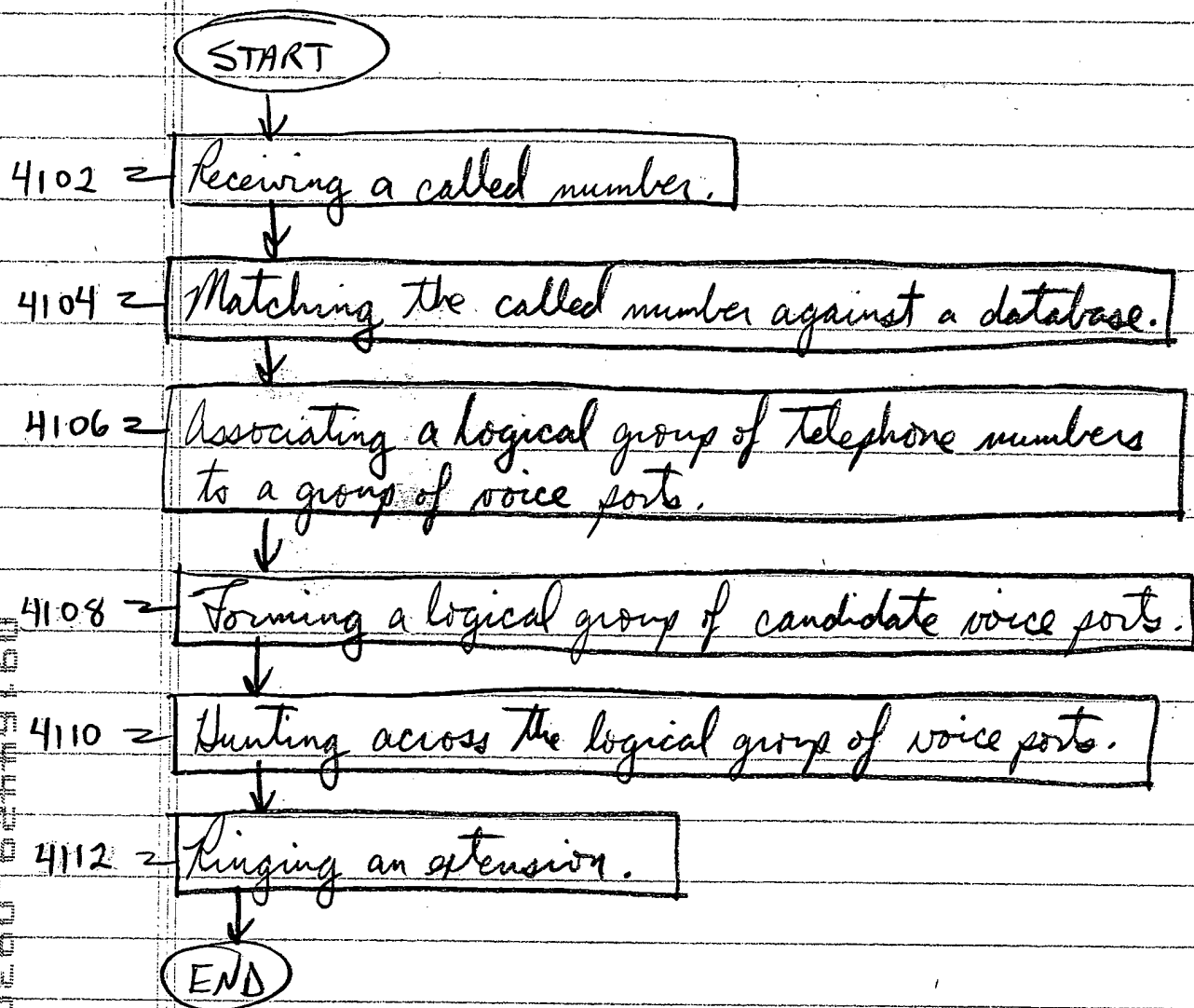


FIGURE 41

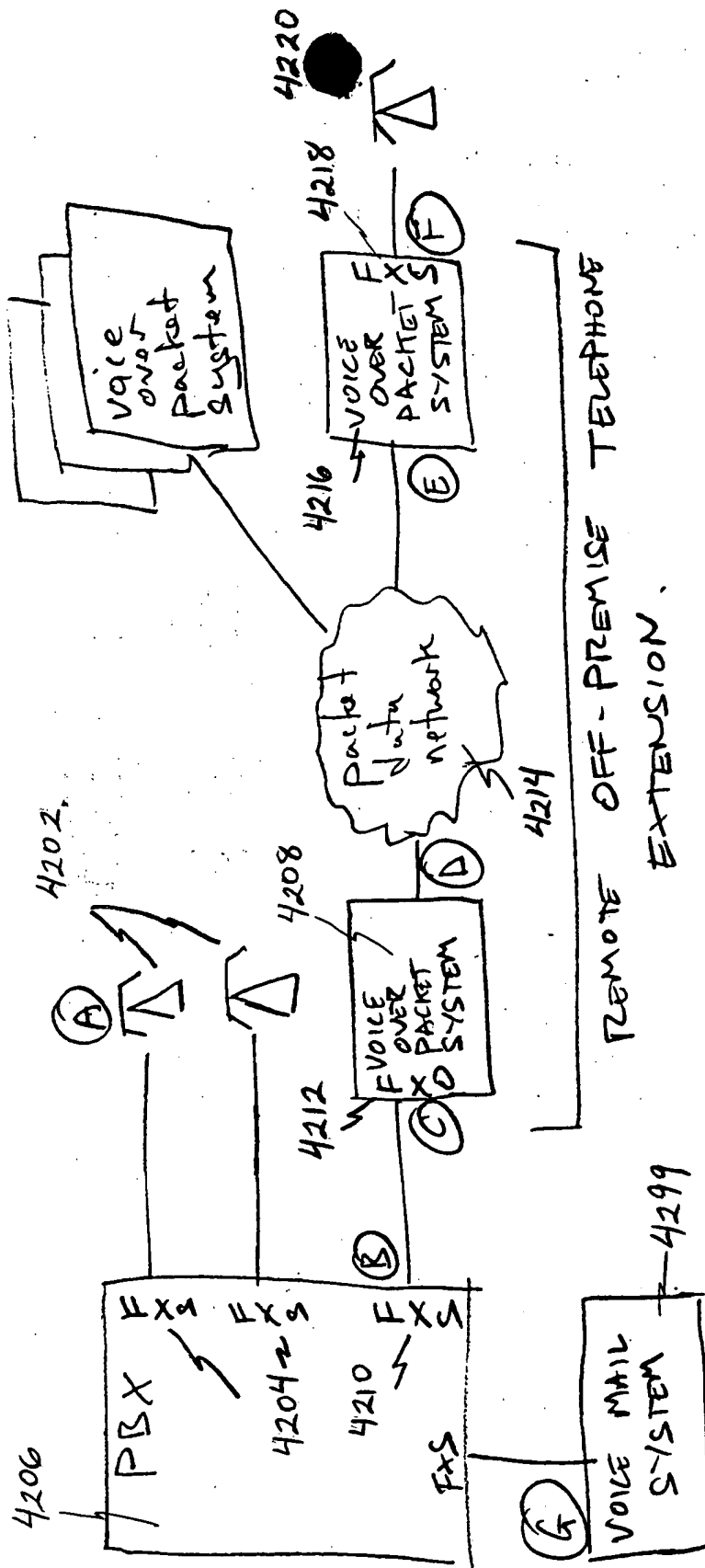


Figure 42

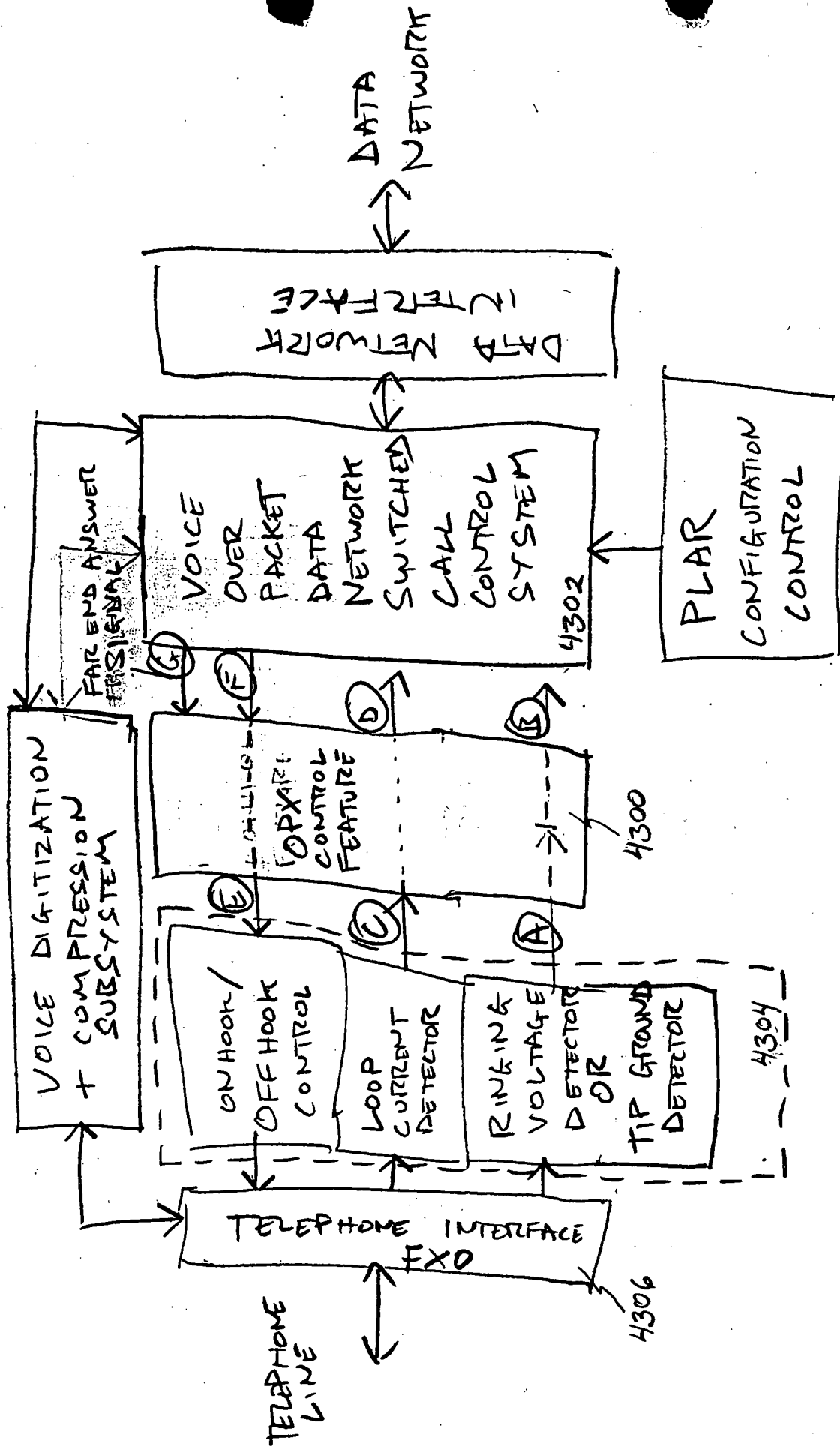


FIGURE 43

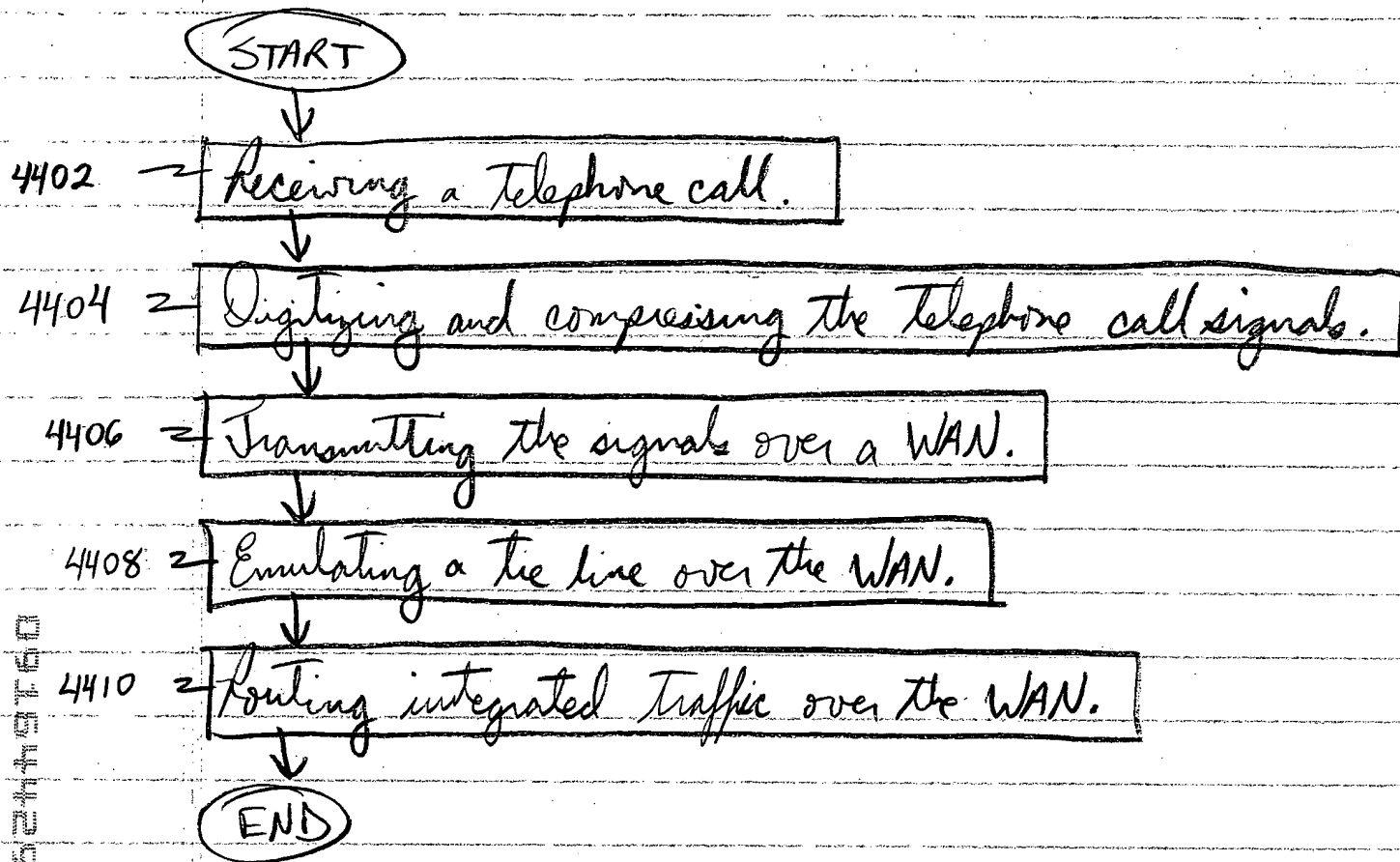


FIGURE 44

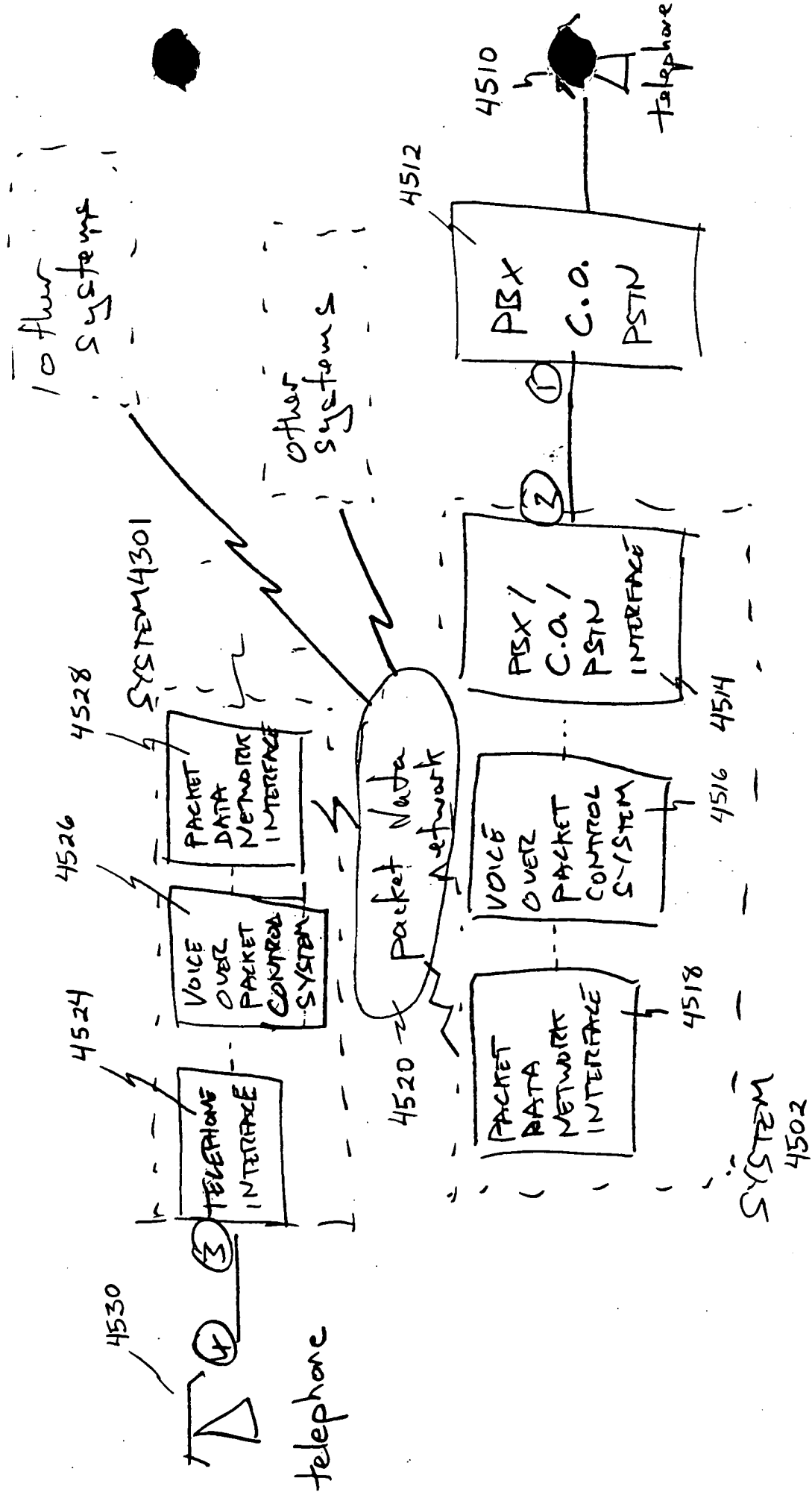


FIGURE 4/5

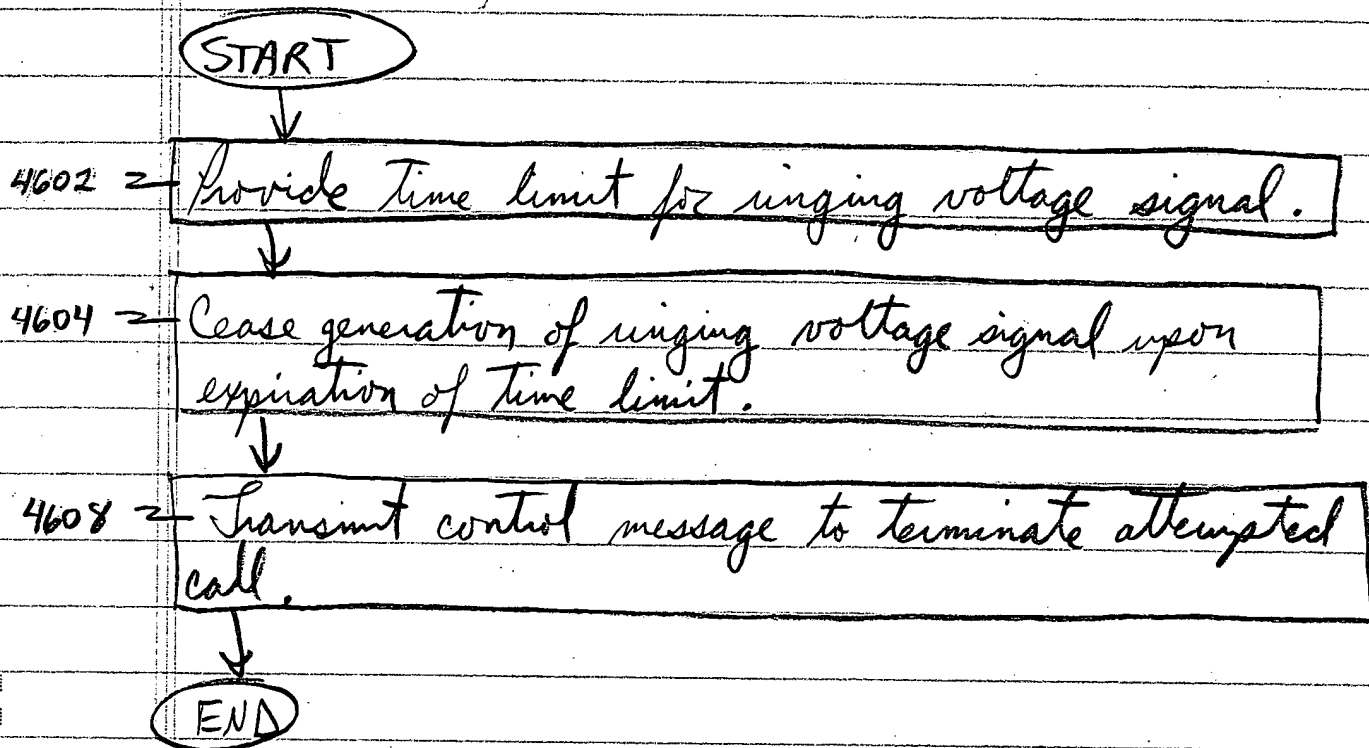


FIGURE 46

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